XRM-ADC-D6-250 /
XRM-ADC-D6-250-AC

Two Channel Data Acquisition Module

User Guide

Version 1.2

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications

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Photo

1. Introduction

The XRM-ADC-D6-250 is a front panel adapter card designed for use with Alpha Data's PMC cards using Virtex 4 and Virtex5 FPGAs.[1]

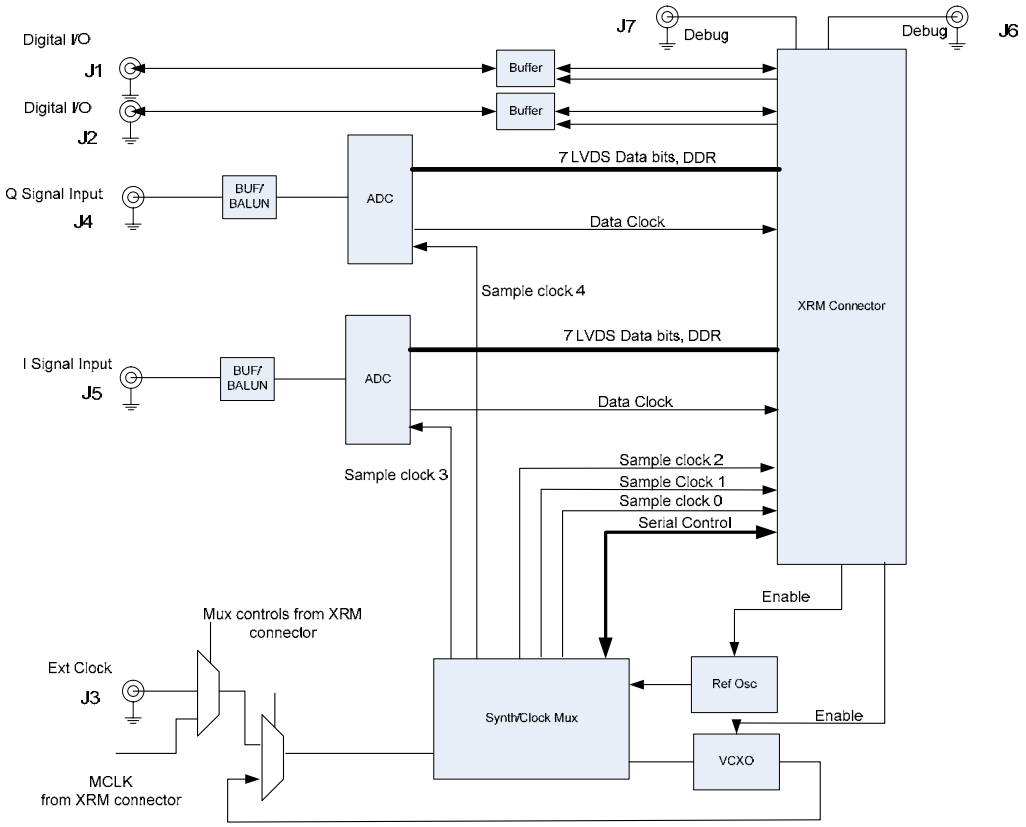
The XRM-ADC-D6-250 provides two dc-coupled channels of analogue to digital conversion with 14 bit resolution and supports sampling rates up to 250 MHz . It is aimed at applications such as IF/Baseband Signal Sampling.

A companion card, the XRM-ADC-D6-250-AC, uses the same ADC architecture but employs a wideband transformer to drive the ADC thus maintaining dynamic performance over a wider bandwidth.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock

Two auxiliary I/O ports are provided for use as trigger inputs and general purpose signalling. A further pair of ports are provided for inter-board connection, fast triggering etc.

[1] Virtex 2 Pro boards (no longer supported) can also be used with this module but cannot make full use of the sampling capabilities of this board. Contact the factory if further information is required.



Where differences between the AC performance and the DC-coupled performance exist, these are explicitly stated. If no such qualification is given then the parameter applies to both versions.

2. Installation

The XRM-ADC-D6-250 is designed to plug in to the front panel connector (SAMTEC QSH series) on an Alpha-Data PMC card. The retaining screws should be tightened to secure the XRM-ADC-D6-250.

Note: This operation should not be performed while the PMC card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

3. Specification

3.1. Inputs

3.1.1. I Signal (J5), Q Signal (J4)

Input:	50 Ohms
Bandwidth (DC version) :	DC to 450 MHz (1dB typ)
Bandwidth (AC version) :	4.5 MHz to 1000 MHz (3 dB)
Level :	+12 dBm (2.5 Vppk =ADC full scale)

3.1.2. Clock In (J3)

Input: 50 Ohms, ac coupled
Level: 0 dBm (630 mV pk to pk) to +12 dBm (2.5V pk to pk) nominal

3.2. Input /Output:

3.2.1. Trig IO Port (J1)

User configurable as input or output
Input: 4k7 Ohms, dc coupled
Level: +3V3 LVTTL or +5V TTL (factory/user selectable[2])

3.2.2. Aux. IO Port (J2)

User configurable as input or output
Input: 4k7 Ohms, dc coupled
Level: +3V3 LVTTL or +5V TTL (factory/user selectable[3])

[2] configured via 0R links
[3] configured via 0R links

4. Options

4.1. Connector type

SMA (7 mm, standard)
Long Barrel SMA (20 mm)
SMB
SMC

4.2. Sample Rate

40 MHz to 250 MHz

4.3. Order Code

XRM-ADC-D6-250 –[Connector option] -[IO voltage option]
XRM-ADC-D6-250-AC –[Connector option] -[IO voltage option]

Fields in square brackets may be omitted in order to obtain the standard configuration for that option. For customisation requirements (e.g. connectors) please contact Alpha Data.

5. Related Documents

ADM-XRC4SX/LX User Manuals
ADM-XRC4FX User Manual
ADPE - 4FX User Manual
ADM-XRC5LX User Manual
ADM-XRC5T1 User Manual
ADM-XRC5T2 User Manual

6. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

7. Pinout

Samtec Pin No.	UCF Name	4LX	4SX	4FX	ADPE4FX	Comments
1	synth_cksel(0)	H28	H28	C27	F35	
2	ref_enab	D32	D32	L28	C34	
3	synth_cksel(1)	H27	H27	C28	G35	
4	vxo_en	C32	C32	K28	D34	
5	synth_ld	K27	K27	L29	F36	
6	synth_sdi	N22	N22	J29	E36	
7	synth_sync	J27	J27	K29	G36	
8	synth_goe	N23	N23	H29	D36	
9	synth_le	H30	H30	F28	E34	
11	synth_sclk	H29	H29	E28	F34	
12	iq_dirn	J29	J29	E29	E37	
13	exttrig	E33	E33	H27	J32	
14	extaux	R21	R21	H30	M32	
15	exttrig_dirn	E32	E32	G27	K32	
16	extaux_dirn	P22	P22	J30	N32	
17	i_enab	C33	C33	G30	N30	
18	i_sck	K28	K28	J26	J37	
19	i_reset_l	C34	C34	F30	M31	
20	i_sdio	K29	K29	K26	J36	
21	i_cs_l	G33	G33	C30	K33	
22	q_cs_l	L31	L31	G26	K34	
23	i_sdo	G32	G32	D30	L33	
24	q_enab	L30	L30	F26	L34	
25	q_sdio	L34	L34	F31	V25	
26	q_sdo	M32	M32	D26	H37	
27	q_sck	L33	L33	G31	W26	
28	q_reset_l	M33	M33	E26	G37	
38	ext_dbug_p	D34	D34	C25	N35	
40	ext_dbug_n	E34	E34	D25	N34	
73	q_chan_data_n(0)	Y33	AK32	D37	T36	
74	q_chan_data_p(1)	T23	AA28	F34	W35	
75	q_chan_data_p(0)	Y32	AK31	E37	U36	
76	q_chan_data_n(1)	U23	AA29	E34	W34	
77	q_chan_data_p(2)	R26	W24	G36	N37	
78	q_chan_data_n(3)	T25	AA30	D36	Y36	
79	q_chan_data_n(2)	T26	Y24	F36	M37	
80	q_chan_data_p(3)	T24	AB30	E36	W36	
81	q_chan_data_n(4)	R29	AE34	K34	V33	
82	q_chan_data_p(5)	N32	AC28	J37	W32	
83	q_chan_data_p(4)	P29	AE33	L34	V34	
84	q_chan_data_n(5)	P32	AB28	J36	Y33	
85	q_chan_data_n(6)	P31	AC30	M31	P37	
86	q_chan_ovr_n	T31	AD32	M32	U35	
87	q_chan_data_p(6)	P30	AC29	N30	R37	
88	q_chan_ovr_p	R31	AE32	N32	V35	
89	q_dck_p	P34	AD34	E32	T30	
91	q_dck_n	R34	AC34	D32	T29	
93	spare1_n	T34	AF34	D27	J34	Note 4
94	spare2_n	U27	AD29	N34	AA24	Note 4
95	spare1_p	T33	AF33	G25	P31	Note 4
96	spare2_p	U26	AE29	M36	AC32	Note 4
97	adcck_p	AG30	AL24	T35	AE36	
99	adcck_n	AG31	AL25	T34	AD36	
102	i_dck_p	AA25	AM21	V37	AE32	
104	i_dck_n	AA26	AM22	U37	AD32	
113	xrm_mckop_n					Note 5
115	xrm_mckop_p					
165	i_chan_data_n(1)	AL34	AM27	Y31	AM36	
166	i_chan_data_n(0)	AF34	AL29	AA23	AN34	
167	i_chan_data_p(1)	AL33	AM26	Y32	AL36	
168	i_chan_data_p(0)	AF33	AL28	AB23	AN35	
169	i_chan_data_n(2)	AH33	AG26	Y26	AJ34	
170	i_chan_data_n(3)	AB23	AN24	AA30	AK32	
171	i_chan_data_p(2)	AH32	AG25	AA26	AH34	

172	i_chan_data_p(3)	AB22	AP24	AA31	AK33	
173	i_chan_data_n(4)	AM33	AF24	AB27	AM35	
174	i_chan_data_n(5)	AK34	AK26	AB25	AN33	
175	i_chan_data_p(4)	AM32	AG23	AB28	AL35	
176	i_chan_data_p(5)	AK33	AL26	AB26	AM33	
177	i_chan_data_n(6)	AH30	AM25	Y29	AN37	
178	i_chan_ovr_n	AL31	AM23	Y27	AG30	
179	i_chan_data_p(6)	AJ30	AN25	AA29	AM37	
180	i_chan_ovr_p	AM31	AL23	AA28	AF30	

Samtec Pin No.	UCF Name	5LX	5T1	5T2	5TZ	Comments
1	synth_cksel(0)	AL6	AP14	Y34	H39	
2	ref_enab	AN4	AA10	J38	G39	
3	synth_cksel(1)	AL5	AN14	AA34	H38	
4	vxo_en	AN5	AB10	K38	G38	
5	synth_ld	AL4	AM13	W35	F40	
6	synth_sdi	AP5	AA8	K40	E39	
7	synth_sync	AM5	AN13	Y35	F39	
8	synth_goe	AP4	AA9	K39	E40	
9	synth_le	AM6	AB8	P37	P37	
11	synth_sclk	AN7	AC8	R37	R37	
12	iq_dirn	AM8	AM12	T37	P38	
13	exttrig	AN8	AC9	N38	M39	
14	extaux	AL10	AL10	W37	L39	
15	exttrig_dirn	AN9	AC10	P38	N39	
16	extaux_dirn	AM10	AL11	W36	M38	
17	i_enab	AP7	AE8	G38	K38	
18	i_sck	AN10	AK11	N39	K40	
19	i_reset_l	AP6	AD9	G39	J38	
20	i_sdio	AM11	AJ11	M39	K39	
21	i_cs_l	AM17	AK9	E40	U38	
22	q_cs_l	AP17	AJ10	W38	W38	
23	i_sdo	AN17	AK8	E39	T37	
24	q_enab	AP16	AJ9	V39	V39	
25	q_sdio	AP12	AE11	F40	AA36	
26	q_sdo	AM15	AH9	M38	AA34	
27	q_sck	AP11	AF11	F39	AA35	
28	q_reset_l	AM16	AH10	L39	Y34	
38	ext_dbug_p	AP9	AD10	H40	H40	
40	ext_dbug_n	AP10	AD11	J40	J40	
73	q_chan_data_n(0)	AH8	AF6	Y40	AA39	
74	q_chan_data_p(1)	AC10	W7	V40	Y37	
75	q_chan_data_p(0)	AG8	AE7	W40	AA40	
76	q_chan_data_n(1)	AD10	V7	W41	AA37	
77	q_chan_data_p(2)	AE9	Y11	U42	P41	
78	q_chan_data_n(3)	AG10	W9	K42	U41	
79	q_chan_data_n(2)	AF9	W11	V41	R40	
80	q_chan_data_p(3)	AF10	W10	J42	T42	
81	q_chan_data_n(4)	AK8	AJ6	Y42	V41	
82	q_chan_data_p(5)	AG11	V8	AA40	V40	
83	q_chan_data_p(4)	AK9	AJ7	W42	U42	
84	q_chan_data_n(5)	AF11	U8	AA39	W41	
85	q_chan_data_n(6)	AH10	AK6	AA41	Y42	
86	q_chan_ovr_n	AE11	V9	P40	AA41	
87	q_chan_data_p(6)	AJ10	AK7	AA42	W42	
88	q_chan_ovr_p	AD11	V10	N40	AA42	
89	q_dck_p	AE8	AG5	Y39	Y39	
91	q_dck_n	AF8	AF5	Y38	Y38	
93	spare1_n	AN13	AF9	T39	T39	Note 4
94	spare2_n	AE4	M8	AL42	AL42	Note 4
95	spare1_p	AC8	Y8	L40	L40	Note 4
96	spare2_p	AC3	L4	AE37	AE37	Note 4
97	adcck_p	AA4	K8	AE40	AE40	
99	adcck_n	AB5	K9	AD40	AD40	
102	i_dck_p	AG1	T8	AV40	AV40	
104	i_dck_n	AG2	U7	AU39	AU39	
113	xrm_mckop_n	fixed	J21	J30	P42	Note 5
115	xrm_mckop_p	fixed	J20	K29	R42	
165	i_chan_data_n(1)	AE1	R8	AD37	AT40	
166	i_chan_data_n(0)	AE3	J7	AM39	AR39	
167	i_chan_data_p(1)	AF1	R7	AD36	AR40	
168	i_chan_data_p(0)	AF3	H7	AL39	AT39	

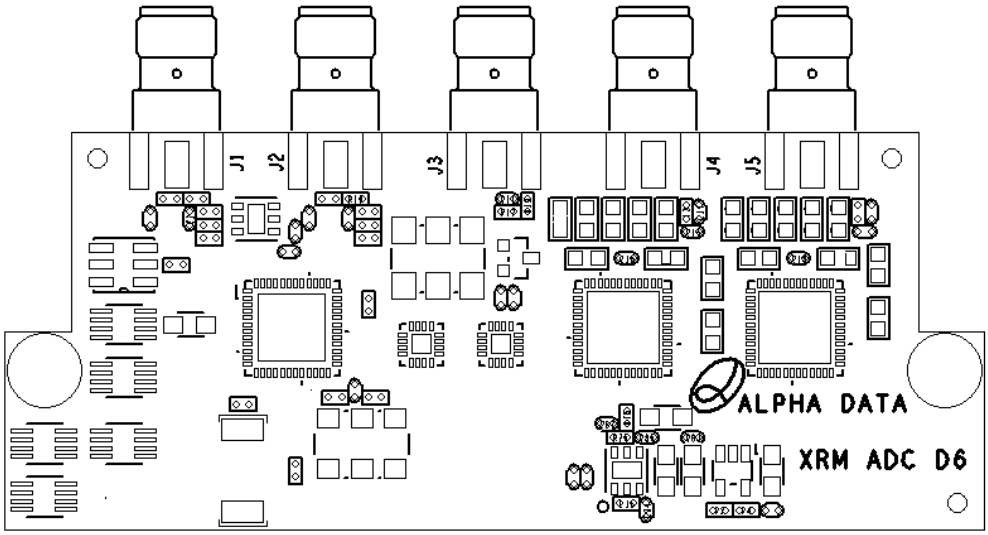
[4] Unused clock pairs (LVDS) from clock generator. Define as "CONFIG PROHIBIT" in UCF.
[5] Programmable clock is routed through FPGA for 5T1, 5T2 and 5TZ; direct to XRM from clock generator on remaining boards

169	i_chan_data_n(2)	AK3	G5	AB36	AK39	
170	i_chan_data_n(3)	AH3	F6	AK39	AH38	
171	i_chan_data_p(2)	AK2	H5	AC35	AJ38	
172	i_chan_data_p(3)	AG3	F5	AJ38	AJ37	
173	i_chan_data_n(4)	AM1	T11	AD35	AM39	
174	i_chan_data_n(5)	AP2	G7	AP40	AP38	
175	i_chan_data_p(4)	AL1	T10	AC36	AL39	
176	i_chan_data_p(5)	AN2	G6	AN40	AN39	
177	i_chan_data_n(6)	AL3	U10	AC34	AM38	
178	i_chan_ovr_n	AN3	E7	AT40	AL37	
179	i_chan_data_p(6)	AM2	T9	AB34	AN38	
180	i_chan_ovr_p	AM3	E6	AR40	AM37	

Analogue data is encoded in 2's complement format, with 0x1FFF (+8191) representing positive full scale and 0x2000 (-8192) representing negative full scale.

OVERRANGE goes high when the signal input is outwith the valid ADC input range.

8. Board Layout



Revision History

Date	Revision	Nature of Change
Jul-2008	1.0	First issue
Feb 2010	1.1	Corrected minor typos
May 2010	1.2	Corrected typo regarding full scale code values. Update/corrected pinout tables. Unsupported boards(XRC2,XPL,XP,XPI) removed. Updated diagrams.