Deployment of 1M-Point FFT on Custom Versal AI-Based Accelerator Card

Introduction

This white paper presents a comprehensive overview of the process of porting AMD's 1-million-point Fast Fourier Transform (FFT) example design from the VCK190 evaluation board to Alpha Data's Versal AI-based ADM-PA100 board. This adaptation involved specific modifications to develop a custom platform and successfully deploy it on the target hardware.

The project builds on AMD's reference design, which is accessible on AMD's GitHub repository for Vitis Tutorials https://github.com/Xilinx/Vitis-Tutorials/tree/2024.1/AI_Engine_Development/AIE/Design_Tutorials/16-1M-Point-FFT-32Gsps. The repository includes both the 1-million-point FFT reference implementation and a bare-metal application for data control and monitoring. Porting this design from the VCK190 to the ADM-PA100 required specific configurations to effectively leverage the ADM-PA100's resources while allowing general usability. Key adaptations involved the creation of a custom platform based on the ADM-PA100's board file and the development of a streamlined workflow that minimized the required modifications for porting. Additionally, the build procedure was adjusted to ensure compatibility with the target hardware while maintaining consistency in deployment scripts.

Performance testing of the adapted design was conducted using the ADM-PA100, booted from a micro-SD card image. Results demonstrated an impressive throughput of 30.72 Gsps for the 1M-point FFT. This high performance was achieved through the advanced AI Engine and hardware acceleration capabilities integral to the Versal AI Engine series architecture, underscoring the ADM-PA100's potential in high-throughput, AI-driven processing applications.

ADM-PA100

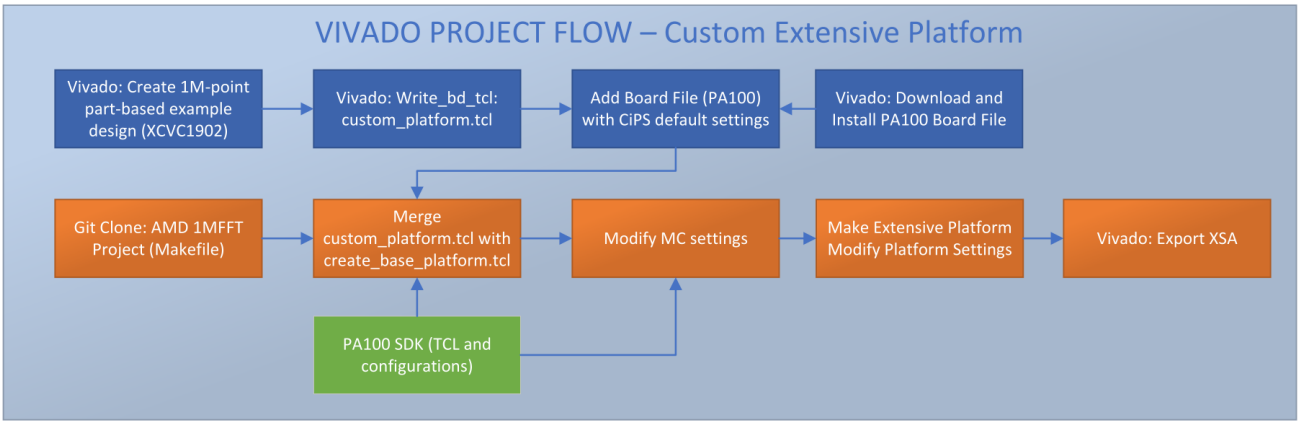
Figure 1 : ADM-PA100

Custom Platform Creation for the ADM-PA100

AMD provides an example design for the VCK190 development board, including Control Interfaces and Processing System (CIPS) and Network-on-Chip (NoC) IP configurations based on the VCK190's board file. However, the board file workflow presents limitations when porting the design to different boards, as the memory controller configuration and pinout requirements can vary significantly across boards. To address this situation, we developed a custom board file and refactored the build scripts to create a platform specifically tailored to the ADM-PA100 board. Additionally, we resolved issues related to TCL scripts specific to the VCK190, which would otherwise obstruct custom platform creation for other boards or devices when using part-based mode.

In summary, AMD's example design was used as a reference, leveraging the part-based approach, and modified to integrate the ADM-PA100's board file. This required customizations across multiple platform elements, such as DDR4 memory controller configuration, reference clocks, and pinouts. By enabling the "extensive platform" option, we identified the platform settings to be passed to Vitis for creating the Vitis platform project. This ensures that the hardware (.xsa) is exported with the appropriate resources—such as AXI ports, clocks, and interrupts—visible in Vitis.

The diagram below ilustrates the steps involved:



Adding 1M-Point FFT Kernels and Runtime Application in Vitis: Building the Extensive Platform

The 1M-Point FFT example provided on GitHub contains everything needed to build the application on the supported platform. However, to run the application on a custom platform, the scripts need to be adapted accordingly.

Key modifications to the build scripts include:

- **Platform Specification**: Scripts are updated to point to the newly created custom platform, rather than the default platform provided in the repository (different .xsa)
- **Vitis Extensive Platform Generation**: A new name is assigned in the scripts to distinguish it from the Vivado custom platform. This serves as the embedded (accelerated) platform where the software will execute. All Makefile references are updated to point to this Vitis platform as well.

The custom platform is configured for the ADM-PA100 board, featuring two distinct execution domains: the AI Engine array, where FFT kernels run, and the Scalar Engines for the PS application (C++), which initiates and monitors the FFT process. This application manages initialization, execution, and data transfer between the AI kernels and external interfaces. The BSP includes bare-metal drivers for data transfer and hardware control, as there is no operating system.

As part of the linking process when running make, a Vivado project is generated, which can then be opened in Vivado for review:

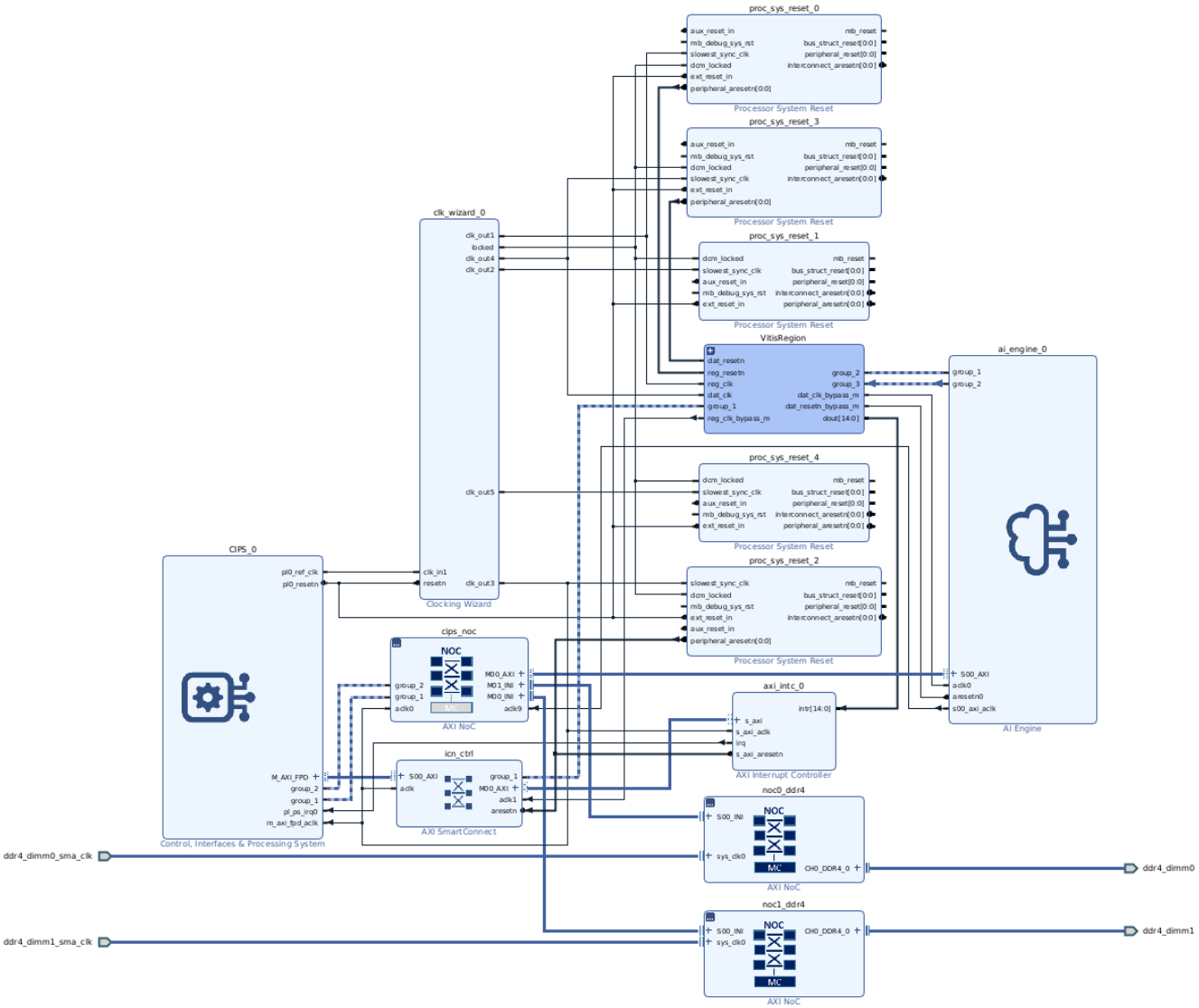


Figure 2 : Vivado IP Integrator Block Diagram of the full platform after including the 1M-Point FFT Kernels in Vitis

For customization, the BSP configuration can be verified to ensure that resource settings, such as the UART port, align with expected values. On the ADM-PA100, the primary UART is preset to monitor program execution.

Running the 1M-Point FFT on the ADM-PA100

Running **make** also generates a package with binaries, including the boot image for the ADM-PA100. At this stage, the .xclbin and BOOT.BIN files can be programmed onto the micro-SD card, enabling the 1M-point FFT to be executed on the board.

Upon boot, the application is expected to run automatically, displaying the FFT results and performance metrics via the serial terminal:

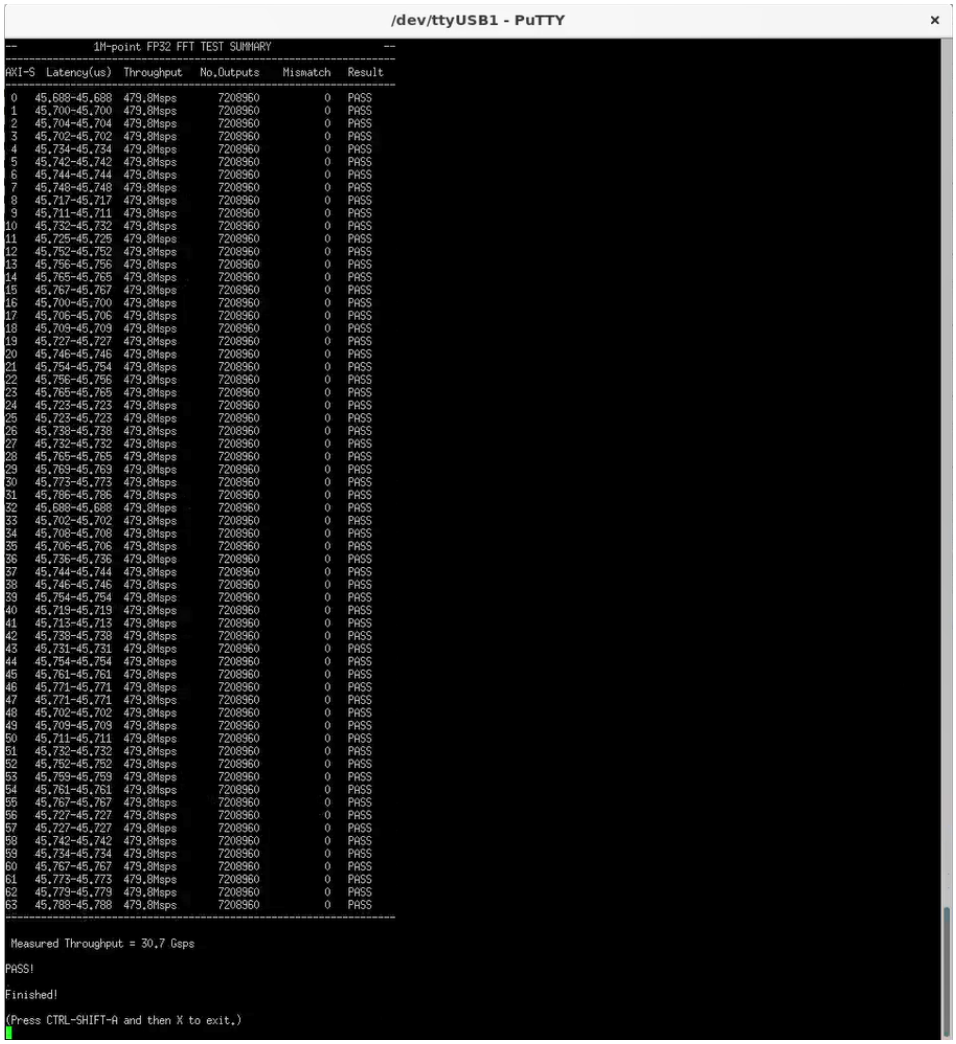


Figure 3 : 1M-Point FFT runtime log showing performance statistics

- **Data Throughput**: The system achieved a data throughput of approximately 30Gsps, demonstrating that the custom platform and application can handle high-speed data processing in real time.
- **Parallel Kernel Execution**: The 64 parallel FFT kernels enabled for efficient computation of the 1M-point FFT, with two independent AXI-S buses per kernel, sourcing 32-bit floating-point samples at a constant average rate of approximately 480 Msps.
- **Real-Time Data Processing**: The application processed data streams in real time using PLIO resources to transfer data between the AI Engine array and PL, demonstrating the Versal ACAP's ability to handle high-throughput, compute-intensive applications.

Conclusions and Summary

This paper demonstrates the feasibility of deploying a high-speed 1-million-point Fast Fourier Transform (FFT) application on a custom Versal ACAP FPGA platform. By creating a custom platform, adapting build scripts, and integrating a bare-metal application, this implementation achieved a performance exceeding 30 Gsps on the ADM-PA100 board. The FFT design utilized 64 parallel kernels to optimize computation and local buffering, with 32 × 6 = 192 AI Engine tiles dedicated to "row transforms" and 32 × 5 = 160 tiles to "column transforms," totaling 352 AI Engine tiles, as outlined in AMD's 1M-Point FFT example design.

This implementation illustrates how a custom board based on the Versal ACAP AI architecture, such as the ADM-PA100, can be effectively utilized for high-performance tasks, making it ideal for real-time signal processing applications.

Revision History

Date	Revision	Nature of Change
20/10/2024	0.1	Draft Release
5/11/2024	1.0	Release

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