ALPHA DATA

ADM-PCIE-KU3 Support & Development Kit Release: 2.0.0

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1 Introduction

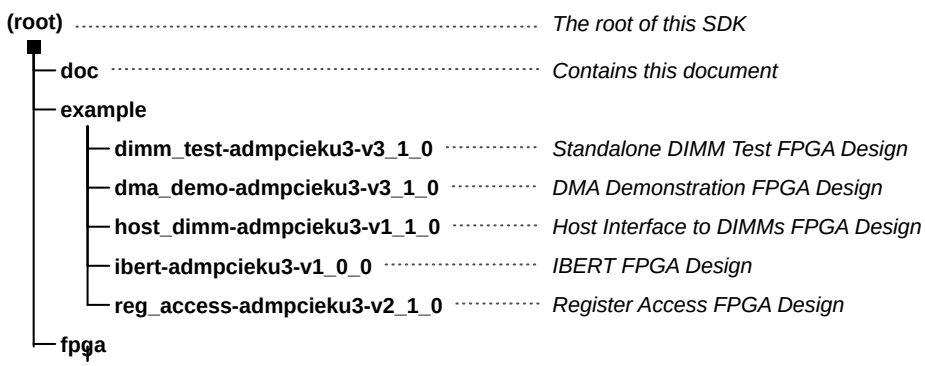
The **ADM-PCIE-KU3 Support & Development Kit (SDK)** is a set of resources for FPGA designers and software engineers working with Alpha Data's ADM-PCIE-KU3 reconfigurable computing card.

The resources of the ADM-PCIE-KU3 SDK include:

- Resources for developing application software for a machine that hosts Alpha Data reconfigurable computing hardware:
  - C/C++ header files and libraries which provide Application Programming Interfaces (APIs) for controlling reconfigurable computing hardware.
  - Documentation about Application Programming Interfaces (APIs) for controlling reconfigurable computing hardware.
  - Common utilities (with source code) for viewing information about reconfigurable computing devices, programming nonvolatile memory, and more.
- Example FPGA designs and host programs (with source code) demonstrating various features of the ADM-PCIE-KU3:
  - The **Standalone DIMM Test FPGA Design**, which demonstrates how to use the Xilinx 7 Series Memory Interface Generator (MIG) IP to create memory controllers for the DDR3 SDRAM SODIMMs in the ADM-PCIE-KU3.
  - The **DMA demonstration FPGA Design**, which demonstrates how to use the DMA engine (AXI4) in Alpha Data's ADM-PCIE-KU3 Board Control and Host Interface IP (ADM-PCIE-KU3-BCHI).
  - The **Host Interface to DIMMs FPGA Design**, which demonstrates combining Alpha Data's ADM-PCIE-KU3 Board Control and Host Interface IP (ADM-PCIE-KU3-BCHI) with the Xilinx Ultrascale Memory Interface Generator (MIG) IP in order to create a host interface that permits access to the DDR3 SDRAM SODIMMs.
  - The **IBERT FPGA Design**, which makes use of the Xilinx IBERT IP to provide ready-to-use IBERT bitstreams that can be used to test the SFP and SATA connectors of the ADM-PCIE-KU3.
  - The **Register Access FPGA Design**, which demonstrates how to use the Direct Slave (AXI4) channel in Alpha Data's ADM-PCIE-KU3 Board Control and Host Interface IP (ADM-PCIE-KU3-BCHI).
- IP and common HDL code provided by Alpha Data:
  - ADM-PCIE-KU3 Board Control and Host Interface IP (ADM-PCIE-KU3-BCHI), which provides a PCI Express to AXI4 interface with a configurable number of DMA engines (AXI4), as well as other features.
  - Common HDL code (i.e. not specific to the ADM-PCIE-KU3), used by the example FPGA designs.

1.1 Structure of this package

The directories making up the ADM-PCIE-KU3 SDK are organised as in Figure 1 below:



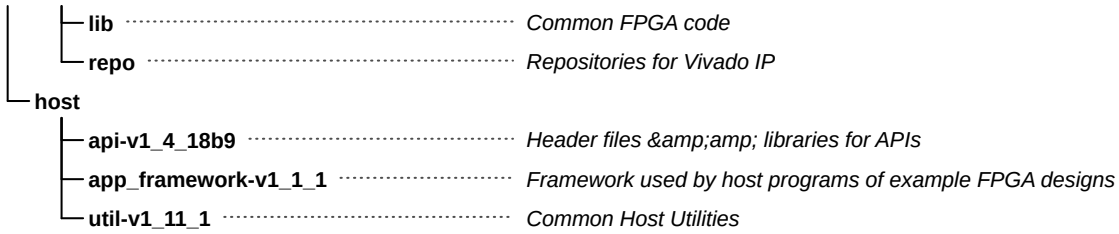


Figure 1 : Structure of the SDK

2 Development operating system support

2.1 Windows

Generally speaking, Alpha Data's Windows software, when supplied in binary form, is compatible with Windows XP and later. However, the choice of Windows operating system used for development mainly depends upon what release of Microsoft Visual Studio and/or Xilinx Vivado are chosen for a project.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore a Windows operating system must be capable of running Vivado. As of writing, Vivado 2017.1 is the current release, and Windows 7 (64-bit) or Windows 10 (64-bit) are recommended.

Vivado path length issue
In Windows, Vivado requires that path lengths of files are no greater than the **MAX_PATH** Win32 constant, which is 260 characters (including the NUL character used to terminate a string). This limit is easily exceeded when a Vivado project uses IP (cores) and the path length of the Vivado project file (.xpr) exceeds about 80 characters. Exceeding the **MAX_PATH** limit can result in otherwise inexplicable failures when implementing an FPGA design in Vivado.

The recommended workaround for this issue is to use the **subst** command to map a drive letter (e.g. **Z:**) to the root of this SDK. If done correctly, the result is the existence of directories **Z:\doc**, **Z:\example**, **Z:\fpga** etc.

When developing software to run on a host machine, Microsoft Visual Studio is likely to be used for building applications. Therefore, the Windows operating system must be capable of running a particular version of Microsoft Visual Studio. For Microsoft Visual Studio 2012 or 2013, Windows 7 or Windows 8 are recommended.

2.2 Linux

Alpha Data generally does not supply binaries for Linux because of the large number of architectures and configurations that exist across various Linux distributions. Source code is provided, however, and can be built for most Linux distributions.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore the supported Linux distributions depend upon the release of Vivado chosen for a project. As of writing, Vivado 2017.1 is the current release and therefore the following Linux distributions are recommended:

- Red Hat Enterprise Server/Workstation 7.2 & 7.3 (64-bit)
- Red Hat Enterprise Workstation 6.6, 6.7 & 6.8 (64-bit)
- SUSE Linux Enterprise 11.4 & 12.2 (64-bit)
- CentOS 7.2 & 7.3 (64-bit)
- CentOS 6.7 & 6.8 (64-bit)
- Ubuntu Linux 16.04.1 LTS (64-bit)

Linux distributions that are not listed might result in Vivado failing to work, or only partially working. They are not supported by Xilinx.

3 Associated documents

(1) Common Host Utilities for Windows & Linux
(root)/host/util-v1_11_1/doc/ad-ug-0055_v1_3.pdf

(2) Common Host Utilities for VxWorks
(root)/host/util-v1_11_1/doc/ad-ug-0086_v1_1.pdf

(3) ADMXRC3 API Specification
(root)/host/api-v1_4_18b9/doc/ad-ug-0003_v1_13.pdf

(4) ADMXRC3 API Hardware Addendum
(root)/host/api-v1_4_18b9/doc/ad-ug-0009_v1_12.pdf

(5) ADM-PCIE-KU3 Standalone DIMM Test FPGA Design
(root)/dimm_test-admpcieku3-v3_1_0/doc/ad-ug-0053_v1_7.pdf

(6) Using Xilinx Ultrascale MIG 7.x with the ADM-PCIE-KU3
(root)/dimm_test-admpcieku3-v3_1_0/doc/ad-ug-0054_v1_4.pdf

(7) ADM-PCIE-KU3 DMA Demonstration FPGA Design
(root)/dma_demo-admpcieku3-v3_1_0/doc/ad-ug-0051_v1_5.pdf

(8) ADM-PCIE-KU3 Host Interface to DIMMs FPGA Design
(root)/example/host_dimm-admpcieku3-v1_1_0/doc/ad-ug-0096_v1_1.pdf

(9) ADM-PCIE-KU3 IBERT FPGA Design
(root)/example/ibert-admpcieku3-v1_0_0/doc/ad-ug-0088_v1_2.pdf

(10) ADM-PCIE-KU3 Register Access FPGA Design
(root)/reg_access-admpcieku3-v2_1_0/doc/ad-ug-0052_v1_3.pdf

(11) IPROG Reconfiguration from Flash Memory on the ADM-PCIE-KU3
(root)/doc/ad-an-0050_v1_0.pdf

4 Release history

4.1 Release 2.0.0

(1) General

(a) 2017.1 is the recommended Xilinx Vivado version for this release of the SDK.

(2) Example FPGA designs

(a) Updated all example FPGA designs for Vivado 2017.1.

(b) For all example FPGA designs, invidual project generation scripts (named **mkxpr-<configuration>.tcl**) no longer close the Vivado project after generating it. Now, after **source**ing such a script using "Tools -> Run Tcl Script..." from the Vivado GUI menu, it can be simulated or implemented without needing to first reopen it.

Bulk project generation scripts (typically named **mkxpr-all.tcl**) still close projects after generating them, to avoid a proliferation of Vivado GUI windows.

(c) The **Standalone DIMM Test FPGA Design** (dimm_test-admpcieku3) now has a behavioral simulation testbench including DDR3 SDRAM chip models, and now has additional configurations for boards fitted with 2 x 16 GiB SODIMMs.

(d) The **DMA Demonstration FPGA Design** (dma_demo-admpcieku3) now has a behavioral simulation testbench which, applies AXI4 stimulus to rest of the design via the master AXI4 interfaces of the **ADM-PCIE-KU3-BCHI** IP instance.

This FPGA design now requires Vivado 2016.3 or later, due to use of ADM-PCIE-KU3-BCHI IP v1.6 (see below, "IP").

(e) The **Register Access FPGA Design** now requires Vivado 2016.3 or later, due to use of ADM-PCIE-KU3-BCHI IP v1.6 (see below, "IP").

(f) New FPGA Design: **Host Interface to DIMMs FPGA Design** (host_dimm-admpcieku3), which demonstrates one way to make the DDR3 SDRAM SODIMMs readable and writable from a host program.

(g) New FPGA Design: **IBERT FPGA design** (ibert-admpcieku3), which provides a Bit Error Rate Test (BERT) for the SFP connectors and the SATA connectors.

(3) IP

(a) This release of the SDK includes and uses ADM-PCIE-KU3-BCHI IP v1.6, for Vivado 2016.3 and later.

By default, ADM-PCIE-KU3-BCHI IP v1.6 uses Receiver Equalization settings that have been found to resolve PCI Express signal integrity issues that have been encountered when the ADM-PCIE-KU3 is used in certain motherboards. The Receiver Equalization settings are configurable via the IP customization GUI for ADM-PCIE-KU3-BCHI IP v1.6.

Vivado 2016.3 or later is required because the Xilinx PCI Express Endpoint IP in Vivado 2016.2 and earlier does not expose Receiver Equalization settings.

(4) Host software

(a) The Common Host Utilities have been updated to version 1.11.0. The relevant fixes and improvements for the ADM-PCIE-KU3 are:

(i) The version of the **flash** utility included in this release of the ADM-PCIE-KU3 SDK resolves "FPGA mismatch" errors seen when using the **flash** utility from ADM-PCIE-KU3 SDK 1.0.0 to program bitstreams into Flash memory on Alpha Data's Ultrascale-based FPGA cards.

(ii) The Common Host Utilities now have common source code for Linux, Windows and VxWorks. However, the method of building them for each supported operating system is different.

(iii) The Common Host Utilities can now also be built for VxWorks as a downloadable kernel module (DKM), as well as for Linux and Windows.

(b) The ADMXRC3 API Header Files have been updated to version 1.8.3, although there are effectively no functional differences for the ADM-PCIE-KU3.

(c) The framework used by test/demonstration programs for example FPGA designs has been updated to version 1.1.1, which includes minor bugfixes and support for several more Alpha Data reconfigurable computing products, but otherwise has no functional differences for the ADM-PCIE-KU3.

4.2 Release 1.0.0

This is the first release of the ADM-PCIE-KU3 Support & Development Kit.

Revision History

Date	Revision	Nature of change
9 Sep 2015	1.0	Initial version.
21 Apr 2017	1.1	Updated for release 2.0.0: New example FPGA design "ibert". New example FPGA design "host_dimm".

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