ALPHA DATA

ADM-PCIE-8K5 Support & Development Kit Release: 2.0.0

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1 Introduction

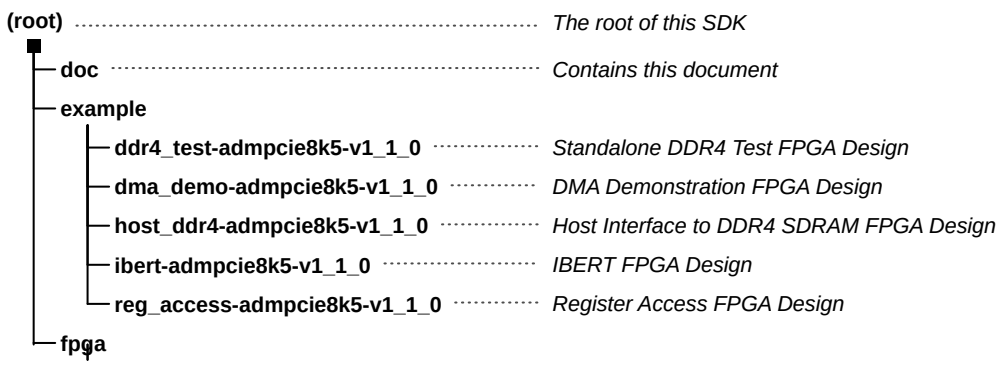
The **ADM-PCIE-8K5 Support & Development Kit (SDK)** is a set of resources for FPGA designers and software engineers working with Alpha Data's ADM-PCIE-8K5 reconfigurable computing card.

The resources of the ADM-PCIE-8K5 SDK include:

- Resources for developing application software for a machine that hosts Alpha Data reconfigurable computing hardware:
  - C/C++ header files and libraries which provide Application Programming Interfaces (APIs) for controlling reconfigurable computing hardware.
  - Documentation about Application Programming Interfaces (APIs) for controlling reconfigurable computing hardware.
  - Common utilities (with source code) for viewing information about reconfigurable computing devices, programming nonvolatile memory, and more.
- Example FPGA designs and host programs (with source code) demonstrating various features of the ADM-PCIE-8K5:
  - The **Standalone DDR4 Test FPGA Design**, which demonstrates how to use the onboard DDR4 SDRAM banks with Xilinx's Ultrascale DDR4 SDRAM IP.
  - The **DMA Demonstration FPGA Design**, which demonstrates how to use the DMA engines (AXI4) in Alpha Data's ADM-PCIE-8K5 Board Control and Host Interface IP (ADM-PCIE-8K5-BCHI).
  - The **Host Interface to DDR4 SDRAM FPGA Design**, which demonstrates combining Alpha Data's ADM-PCIE-8K5 Board Control and Host Interface IP (ADM-PCIE-8K5-BCHI) with the Xilinx Ultrascale DDR4 SDRAM IP in order to create a host interface that permits access to the on-board DDR4 SDRAM banks.
  - The **IBERT FPGA Design**, which makes use of the Xilinx IBERT IP to provide ready-to-use IBERT bitstreams that can be used to test the QSFP and FireFly connectors of the ADM-PCIE-8K5.
  - The **Register Access FPGA Design**, which demonstrates how to use the Direct Slave (AXI4) channel in Alpha Data's ADM-PCIE-8K5 Board Control and Host Interface IP (ADM-PCIE-8K5-BCHI).
- IP and common HDL code provided by Alpha Data:
  - ADM-PCIE-8K5 Board Control and Host Interface IP (ADM-PCIE-8K5-BCHI), which provides a PCI Express to AXI4 interface with a configurable number of DMA engines (AXI4), as well as other features.
  - Common HDL code (i.e. not specific to the ADM-PCIE-8K5), used by the example FPGA designs.

1.1 Structure of this package

The directories making up the ADM-PCIE-8K5 SDK are organised as in Figure 1 below:



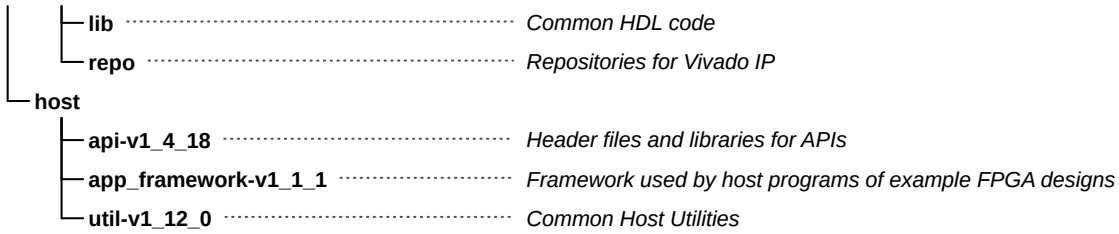


Figure 1 : Structure of the SDK

2 Development operating system support

2.1 Windows

Generally speaking, Alpha Data's Windows software, when supplied in binary form, is compatible with Windows XP and later. However, the choice of Windows operating system used for development mainly depends upon which releases of Microsoft Visual Studio and/or Xilinx Vivado are chosen for a project.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore a Windows operating system must be capable of running Vivado. As of writing, Vivado 2017.2 is the current release, and Windows 7 SP1 and Windows 10 are recommended.

Vivado path length issue
In Windows, Vivado requires that path lengths of files are no greater than the **MAX_PATH** Win32 constant, which is 260 characters (including the NUL character used to terminate a string). This limit is easily exceeded when a Vivado project uses IP (cores) and the path length of the Vivado project file (.xpr) exceeds about 80 characters. Exceeding the **MAX_PATH** limit can result in otherwise inexplicable failures when implementing an FPGA design in Vivado.

The recommended workaround for this issue is to use the **subst** command to map a drive letter (e.g. **Z:**) to the root of this SDK. If done correctly, the result is the existence of directories **Z:\doc**, **Z:\example**, **Z:\fpga** etc.

When developing software to run on a host machine, Microsoft Visual Studio is likely to be used for building applications. Therefore, the Windows operating system must be capable of running a particular version of Microsoft Visual Studio. For Microsoft Visual Studio 2012 or 2013, Windows 7, Windows 8.1 and Windows 10 are recommended.

2.2 Linux

Alpha Data generally does not supply binaries for Linux because of the large number of architectures and configurations that exist across various Linux distributions. Source code is provided, however, and can be built for most Linux distributions.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore the supported Linux distributions depend upon the release of Vivado chosen for a project. As of writing, Vivado 2017.2 is the current release and therefore the following Linux distributions are recommended:

- Red Hat Enterprise Workstation / Server 7.2 & 7.3 (64-bit)
- Red Hat Enterprise Workstation 6.6, 6.7 & 6.8 (64-bit)
- CentOS 6.7, 6.8, 7.2 & 7.3 (64-bit)
- SUSE Linux Enterprise 11.4 & 12.2 (64-bit)
- Ubuntu Linux 16.04.1 LTS (64-bit)

Linux distributions that are not listed might result in Vivado failing to work, or only partially working. They are not supported by Xilinx.

3 Associated documents

(1) Common Host Utilities for Windows & Linux
(root)/host/util-v1_12_0/doc/ad-ug-0055_v1_4.pdf

(2) Common Host Utilities for VxWorks
(root)/host/util-v1_12_0/doc/ad-ug-0086_v1_2.pdf

(3) ADMXRC3 API Specification
(root)/host/api-v1_4_18/doc/ad-ug-0003_v1_13.pdf

(4) ADMXRC3 API Hardware Addendum
(root)/host/api-v1_4_18/doc/ad-ug-0009_v1_12.pdf

(5) ADM-PCIE-8K5 Standalone DDR4 Test FPGA Design
(root)/example/ddr4_test-admpcie8k5-v1_1_0/doc/ad-ug-0074_v1_2.pdf

(6) Using Xilinx Ultrascale MIG with the ADM-PCIE-8K5
(root)/example/ddr4_test-admpcie8k5-v1_1_0/doc/ad-ug-0075_v1_2.pdf

(7) ADM-PCIE-8K5 DMA Demonstration FPGA Design
(root)/example/dma_demo-admpcie8k5-v1_1_0/doc/ad-ug-0073_v1_2.pdf

(8) ADM-PCIE-8K5 Host Interface to DDR4 SDRAM FPGA Design
(root)/example/host_ddr4-admpcie8k5-v1_1_0/doc/ad-ug-0098_v1_2.pdf

(9) ADM-PCIE-8K5 IBERT FPGA Design
(root)/example/ibert-admpcie8k5-v1_1_0/doc/ad-ug-0087_v1_2.pdf

(10) ADM-PCIE-8K5 Register Access FPGA Design
(root)/example/reg_access-admpcie8k5-v1_1_0/doc/ad-ug-0076_v1_2.pdf

(11) IPROG Reconfiguration from Flash Memory on the ADM-PCIE-8K5
(root)/doc/ad-an-0052_v1_0.pdf

4 Release history

4.1 Release 2.0.0

(1) General

(a) 2017.2 is the recommended Xilinx Vivado version for this release of the SDK.

(2) Example FPGA designs

(a) Updated all example FPGA designs for Vivado 2017.2.

(b) For all example FPGA designs, invidual project generation scripts (named **mkxpr-<configuration>.tcl**) no longer close the Vivado project after generating it. Now, after **source**ing such a script using "Tools -> Run Tcl Script..." from the Vivado GUI menu, it can be simulated or implemented without needing to first reopen it.

Bulk project generation scripts (typically named **mkxpr-all.tcl**) still close projects after generating them, to avoid a proliferation of Vivado GUI windows.

(c) New FPGA Design: **Host Interface to DDR4 SDRAM FPGA Design** (host_ddr4-admpcie8k5), which demonstrates one way to make the on-board banks of DDR4 SDRAM readable and writable from a host program.

(d) New FPGA Design: **IBERT FPGA Design** (ibert-admpcie8k5), which provides a Bit Error Rate Test (BERT) for the QSFP connectors and the FireFly connectors.

(3) IP

(a) This release of the SDK includes and uses **ADM-PCIE-8K5-BCHI IP** v1.2, for Vivado 2016.3 and later. This means that the example FPGA designs **dma_demo**, **host_ddr4** and **reg_access** now require Vivado 2016.3 or later.

(4) Host software

(a) The Common Host Utilities have been updated to version 1.12.0:

- The Common Host Utilities can now also be built for VxWorks, from the same source code.
- Updated the **avr2util** microcontroller maintenance utility from version 1.9.0 to 2.7.1, which adds several new commands and support for communicating with the microcontroller via USB (since **avr2util** version 2.0.0).

(b) The ADMXRC3 API Header Files have been updated v1.8.3, although there are no functional differences for the ADM-PCIE-8K5.

(c) Added AVR2 API Header Files, used by the **avr2util** utility.

(d) The framework used by test/demonstration programs for example FPGA designs has been updated to version 1.1.1. This corrects a bug in the method **CExAppNumParse::ParseUIntHex64** in **exappnumparse.h**, which resulted in incorrect values being returned.

4.2 Release 1.0.0

This is the first release of the ADM-PCIE-8K5 Support & Development Kit.

Revision History

Date	Revision	Nature of change
11th May 2016	1.0	Initial version.
30th Jun 2017	1.1	Updated for release 2.0.0; see Release history.

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