



ALPHA DATA

**ADM-PCIE-9V3 Support &
Development Kit
Release: 1.2.0**

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1 Introduction

The **ADM-PCIE-9V3 Support & Development Kit (SDK)** is a set of resources for FPGA designers and software engineers working with Alpha Data's ADM-PCIE-9V3 reconfigurable computing card. The latest version of the ADM-PCIE-9V3 SDK can be found at:

https://support.alpha-data.com/Downloads.aspx?fldr_req=Downloads/admpcie9v3/sdk

The resources of the ADM-PCIE-9V3 SDK include:

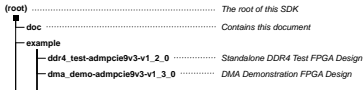
- Resources for developing application software for a machine that hosts Alpha Data reconfigurable computing hardware, using the **ADXDMA Driver**:
 - C/C++ header files and libraries which provide Application Programming Interfaces (APIs).
 - Documentation about Application Programming Interfaces (APIs).
 - Utilities (with source code), which make use of the Application Programming Interfaces (APIs).
- Example FPGA designs and host programs (with source code) demonstrating various features of the ADM-PCIE-9V3:
 - The **Standalone DDR4 Test FPGA Design**, which demonstrates how to use the onboard DDR4 SDRAM with Xilinx's Ultrascale DDR4 SDRAM IP.
 - The **DMA Demonstration FPGA Design**, which demonstrates high performance DMA using the Xilinx XDMA (PCI Express) IP together with Alpha Data's **ADXDMA Driver**.
 - The **Host Interface to DDR4 SDRAM FPGA Design**, which demonstrates combining the Xilinx XDMA (PCI Express) IP with the Xilinx Ultrascale DDR4 SDRAM IP in order to create a host interface that permits access to the on-board DDR4 SDRAM.

A host program that uses the **ADXDMA Driver** demonstrates high performance DMA data transfer between host memory and the DDR4 SDRAM.

- Host Interface to SPI Flash Design**
Demonstrates combining the Xilinx XDMA (PCI Express) IP with the Xilinx AXI SPI IP in order to create a host interface that permits the host CPU to access the on-board SPI Flash that is used to configure the FPGA.
The **ADXDMA Driver** includes a utility `adxdma_spi` that allows the host CPU to erase, program and verify SPI Flash chips via the Xilinx AXI SPI IP.
- The **IBERT FPGA Design**, which makes use of the Xilinx IBERT IP to provide ready-to-use IBERT bitstreams that can be used to test the QSFP and OpenCAPI connectors of the ADM-PCIE-9V3.
- IP and common HDL code provided by Alpha Data:
 - ADM-PCIE-9V3 Board Control Interface IP (ADM-PCIE-9V3-BCI), which provides an AXI4 Lite interface to the board's microcontroller, among other functions.
 - Common HDL code (i.e. not specific to the ADM-PCIE-9V3), used by the example FPGA designs.

1.1 Structure of this package

The directories making up the ADM-PCIE-9V3 SDK are organised as in [Figure 1](#) below:



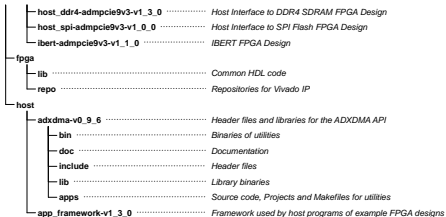


Figure 1 : Structure of the SDK

1.2 The ADXDMA Driver

The **ADXDMA Driver** is a kernel-mode driver for the PCI Express Endpoint in the Xilinx XDMA IP, which provides a user-mode application programming interface (API). The latest version can be found here:

(Windows) https://support.alpha-data.com/Downloads.aspx?fldr_req=Downloads/adxdma

(Linux) TBA

2 Recommended Vivado versions

For this release of the ADM-PCIE-9V3 SDK, use of the Xilinx Vivado toolset version 2017.1 to 2018.3 (inclusive) is generally recommended for building and simulating the example FPGA designs. However, some of the example FPGA designs are subject to known issues, which affect the recommended Vivado version.

Recommended Vivado versions for the example FPGA designs are as follows:

Example FPGA design	Short name	Recommended Vivado version
Standalone DDR4 SDRAM Test FPGA Design	ddr4_test	2018.3
DMA Demonstration FPGA Design	dma_demo	2018.3
Host Interface to DDR4 SDRAM FPGA Design	host_ddr4	2018.3
Host Interface to SPI Flash FPGA Design	host_spi	ES1
IBERT FPGA Design	ibert	2018.3

Table 1 : Recommended Vivado version by example FPGA design

Please refer to the documentation for each example FPGA design for further details of any known issues that affect them.

3 Development operating system support

3.1 Windows

Generally speaking, Alpha Data's Windows software, when supplied in binary form, is compatible with Windows XP and later. However, the choice of Windows operating system used for development mainly depends upon which releases of Microsoft Visual Studio and/or Xilinx Vivado are chosen for a project.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore a Windows operating system must be capable of running Vivado. As of writing, Vivado 2018.3 is the current release, and as per the [Vivado 2018.3 release notes](#), Windows 7 SP1 and Windows 10 are recommended.

Vivado path length issue

In Windows, Vivado requires that path lengths of files are no greater than the **MAX_PATH** Win32 constant, which is 260 characters (including the NUL character used to terminate a string). This limit is easily exceeded when a Vivado project uses IP (cores) and the path length of the Vivado project file (.xpr) exceeds about 80 characters. Exceeding the **MAX_PATH** limit can result in otherwise inexplicable failures when implementing an FPGA design in Vivado.

The recommended workaround for this issue is to use the **subst** command to map a drive letter (e.g. **Z:**) to the root of this SDK. If done correctly, the result is the existence of directories **Z:\doc**, **Z:\example**, **Z:\fpga** etc.

When developing software to run on a host machine, Microsoft Visual Studio is likely to be used for building applications. Therefore, the Windows operating system must be capable of running a particular version of Microsoft Visual Studio. For Microsoft Visual Studio 2017, Windows 7, Windows 8.1 and Windows 10 are recommended.

3.2 Linux

Alpha Data generally does not supply binaries for Linux because of the large number of architectures and configurations that exist across various Linux distributions. Source code is provided, however, and can be built for most Linux distributions.

When developing an FPGA design, the Xilinx Vivado toolset is used, and therefore the supported Linux distributions depend upon the version of Vivado chosen for a project. As of writing, Vivado 2018.3 is the latest version, and as per the [Vivado 2018.3 release notes](#), the following Linux distributions are recommended:

- Red Hat Enterprise Workstation / Server 7.2 to 7.5 (64-bit)
- Red Hat Enterprise Workstation 6.6 to 6.9 (64-bit)
- CentOS 6.7 to 6.9 or 7.2 to 7.5 (64-bit)
- SUSE Linux Enterprise 11.4 & 12.3 (64-bit)
- Ubuntu Linux 16.04.4 LTS or 18.04 LTS (64-bit)

Linux distributions that are not listed might result in Vivado failing to work, or only partially working. They are not supported by Xilinx.

4 Associated documents

- (1) ADXDMA API
(root)/host/adxdma-v0_9_6/doc/ad-ug-0105_v1_3.pdf
- (2) ADXDMA Board Control API
(root)/host/adxdma-v0_9_6/doc/ad-ug-0112_v1_2.pdf
- (3) ADXDMA Driver Utilities
(root)/host/adxdma-v0_9_6/doc/ad-ug-0110_v1_3.pdf
- (4) ADM-PCIE-9V3 Standalone DDR4 Test FPGA Design
(root)/example/ddr4_test-admpcie9v3-v1_2_0/doc/ad-ug-0099_v1_4.pdf
- (5) Using Xilinx Ultrascale+ MIG with the ADM-PCIE-9V3
(root)/example/ddr4_test-admpcie9v3-v1_2_0/doc/ad-ug-0100_v1_4.pdf
- (6) ADM-PCIE-9V3 DMA Demonstration FPGA Design
(root)/example/dma_demo-admpcie9v3-v1_3_0/doc/ad-ug-0103_v1_4.pdf
- (7) ADM-PCIE-9V3 Host Interface to DDR4 SDRAM FPGA Design
(root)/example/host_ddr4-admpcie9v3-v1_3_0/doc/ad-ug-0109_v1_3.pdf
- (8) ADM-PCIE-9V3 Host Interface to SPI Flash FPGA Design
(root)/example/host_spi-admpcie9v3-v1_0_0/doc/ad-ug-0129_v1_0.pdf
- (9) ADM-PCIE-9V3 IBERT FPGA Design
(root)/example/ibert-admpcie9v3-v1_1_0/doc/ad-ug-0101_v1_3.pdf

5 Release history

5.1 Release 1.0.0

This is the first release of the ADM-PCIE-9V3 Support & Development Kit.

5.2 Release 1.1.0

Enhancement:

- The demonstration programs for the example FPGA designs can now also be built for and run in Linux, after installing the [ADXDMA Driver for Linux](#).
- As of this release of the SDK, the ADXDMA API header files in `host/adxdma-<version>/include` are compatible with Linux as well as Windows. They can be used to develop host programs that use the [ADXDMA Driver for Linux](#).

5.3 Release 1.2.0

Enhancement:

- Updated all example FPGA designs for Vivado 2018.3. The pre-built bitstreams in this release of the SDK were generated using Vivado 2018.3.
- All example FPGA designs now have Tcl scripts, whose filenames are of the form `flash-*.tcl`, for programming the SPI Flash memory with a bitstream using Vivado Hardware Manager. Previously, only those designs which have a PCI Express endpoint had such Tcl scripts.
- For all example FPGA designs, when the project creation scripts, whose filenames are of the form `mkxpr-*.tcl` are invoked in Vivado running in Linux, they no longer attempt to set simulation properties for the **ActiveHDL** simulator. This is because **ActiveHDL** is available only for Windows, and a Tcl script that attempts to set properties for it in the Linux version of Vivado will error out.
- Added a new example FPGA design, **Host Interface to SPI Flash FPGA Design**.
- Added a workaround for a routing failure, seen in in Vivado 2018.2 or later, when implementing the Tandem-enabled design configuration of the **DMA Demonstration FPGA Design**.
- Added I2C functionality to the **IBERT FPGA Design**, which permits access to the module management interfaces of any QSPF+ modules fitted to an ADM-PCIE-9V3.
- The ADXDMA Driver header files and DLL import libraries used by the host programs of example FPGA designs now correspond to ADXDMA Driver 0.9.6 (previously 0.8.0). Similarly, the ADXDMA Driver Utilities included in this release correspond to ADXDMA Driver 0.9.6 (previously 0.8.0).

Revision History

Date	Revision	Nature of change
12th April 2018	1.0	Initial version for Release 1.0.0.
25th May 2018	1.1	Updated for Release 1.1.0.
5th March 2019	1.2	Updated for Release 1.2.0.