ALPHA DATA

ADM-SDEV-CFG1
User Manual

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1 Introduction

The **ADM-SDEV-CFG1** configuration module **board** forms part of the ADA-SDEV-KIT1 space FPGA development kit.

The ADM-SDEV-CFG1 board connects to the configuration FMC socket of the ADM-SDEV-BASE board, allowing the Xilinx tools to interrogate and configure its FPGA.

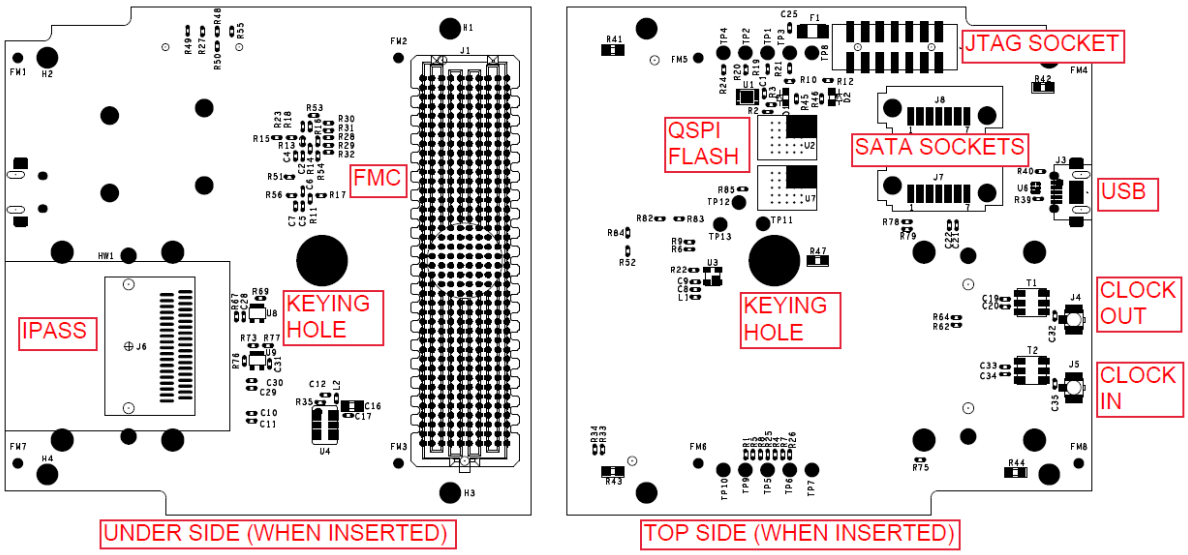

Figure 1 : ADM-SDEV-CFG1 Top and Bottom Views

1.1 Key Features

Key Features

- 1x FMC form factor configuration interface
- 2x 256MB QSPI Flash devices, connected to the configuration bank of the Base board FPGA
- IPASS Connector, allowing remote PCIe connection to the Base board FPGA
- A JTAG header to allow Vivado Hardware Manager configuration and debug
- USB connection to the Base boards system monitor, to allow reporting of system monitor values
- 2x SATA sockets, allows access to 2 high speed serial lanes of the Base board FPGA.
- Fixed LVDS clock output to the Base board FPGA.
- 2x UFL connectors, allows an external clock to be transmitted / received / looped back by the Base board FPGA.
- GPIO loopbacks on the remaining FMC signals.

1.2 References & Specifications

ANSI/VITA 57.1	*FPGA Mezzanine Card (FMC) Standard*, July 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 57.4	*FPGA Mezzanine Card Plus(FMC+) Standard*, March 2016, VITA, Draft

Table 1 : References

2 Installation

2.1 Software Installation

Please refer to the ADA-SDEV-KIT1 area on the Alpha-Data support site for access to system monitoring utilities, documentation and FPGA reference designs.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2.2 Configuration FMC Board

Prior to applying power to the ADM-SDEV-BASE board, the ADM-SDEV-CFG1 board should be fitted into the Config FMC Socket (J2).

it is recommended that the PMC keying pillar should be fitted to the ADM-SDEV-BASE board. This will ensure that only an ADM-SDEV-CFG1 can be fitted to the config FMC Socket.

3 Functional Description

3.1 Overview

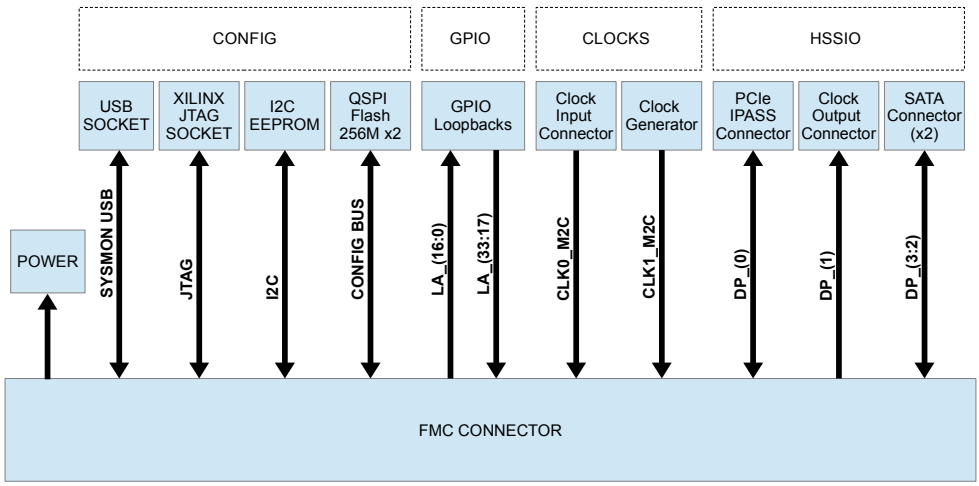

Figure 2 : ADM-SDEV-CFG1 Block Diagram

3.1.1 LED Definitions

The position and description of the board status LED is shown in LED Locations:

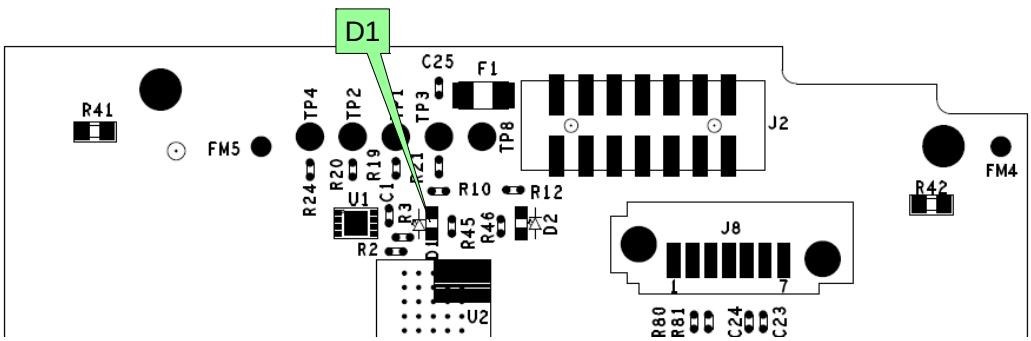

Figure 3 : LED Locations

Comp. Ref.	Function	ON State	Off State
D1(Green)	3.3V Supply Status	Normal operation	Power Off

Table 2 : LED Definitions

3.2 JTAG Interface

3.2.1 On-board Interface

The JTAG boundary scan chain can be accessed via a standard header (J2).

This allows the connection of the Xilinx JTAG cable for FPGA debug and QSPI Flash programming via the Xilinx toolchain.

The JTAG chain starts on the config FMC board and through the Base board, passing through the FPGA, the LPC FMC (if fitted) and the FMC+ (if fitted).

The scan chain is shown in JTAG Boundary Scan Chain:

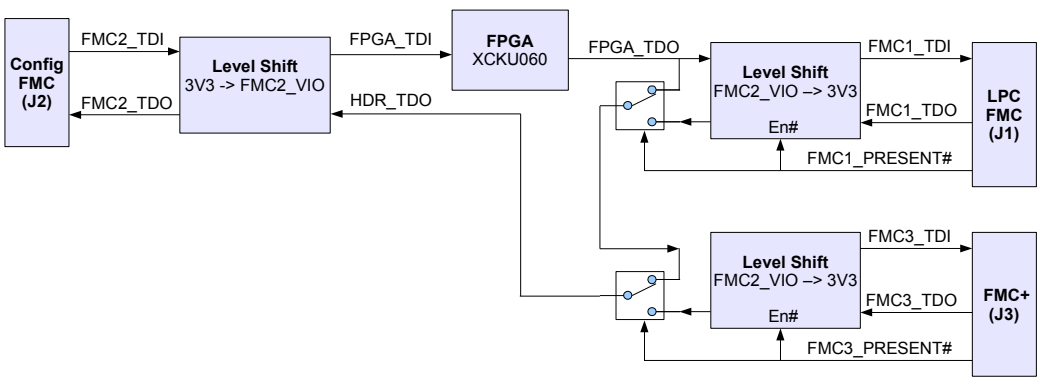

Figure 4 : JTAG Boundary Scan Chain

3.2.2 JTAG Voltages

The Vcc supply provided to the JTAG cable on the config header is +3.3V and is protected by a poly fuse rated at 375mA.

The voltage level of the JTAG chain on the ADM-SDEV-BASE board is set to the config FMC adjustable voltage FMC2_VIO.

3.3 Clocks

The **ADM-SDEV-CFG1** board can provide two different clock sources to the Base board FPGA.

One clock source is generated by an on board oscillator and the other can be input via connector J4.

Source	Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
External (J5)	CLK2_M2C_0	Variable	Bank 24	LVDS	AM32	AN32
Oscillator	CLK2_M2C_1	150MHz Fixed	Bank 24	LVDS	AM31	AN31

Table 3 : Input CLK_M2C Connections

The **ADM-SDEV-CFG1** board can also output a clock signal via connector J4.

This clock is generated by the FPGA on the base board.

Source	Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
FPGA	DP1_C2M_1	Variable	MGT Quad 224	LVDS	AV6	AV5

Table 4 : Output Clock Connection

3.4 IPASS Connector

One of the high speed serial lanes is connected to an IPASS connector for remote PCIe connection.

Connector	Signal	FPGA Bank	"P" pin	"N" pin
IPASS (J6)	DP0_C2M	MGT Quad 224	AW8	AW7
	DP0_M2C	MGT Quad 224	AW4	AW3
	GBTCLK0_M2C	MGT Quad 224	AT10	AT9

Table 5 : IPASS PCIe Connections

3.5 SATA Connectors

The ADM-SDEV-CFG1 board has two standard right angle SATA receptacles for use with SATA compliant storage devices.

Connector	Signal	FPGA Bank	"P" pin	"N" pin
SATA_1 (J7)	DP2_C2M	MGT Quad 224	AU8	AU7
	DP2_M2C	MGT Quad 224	AU4	AU3
SATA_2 (J8)	DP3_C2M	MGT Quad 224	A16	A15
	DP3_M2C	MGT Quad 224	A12	A11

Table 6 : SATA Connections

3.6 Health Monitoring

The **ADM-SDEV-BASE** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Atmel AVR microcontroller.

The system monitor microcontroller can be accessed via the USB connector (J3), please refer to the

ADM-SDEV-BASE user manual for more information.

3.7 GPIO Loopback

Many of the unused FMC GPIO signals are looped back on the ADM-SDEV-CFG1 board for test purposes.

Revision History

Date	Revision	Nature of Change
12 Sep 2018	0.1	Initial Draft
21 Nov 2018	0.2	Updated LED definition
27 Nov 2018	1.0	First Release
13 May 2019	1.1	Removed reference to CDROM in section 2.1
18 Mar 2020	1.2	Corrected typos

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