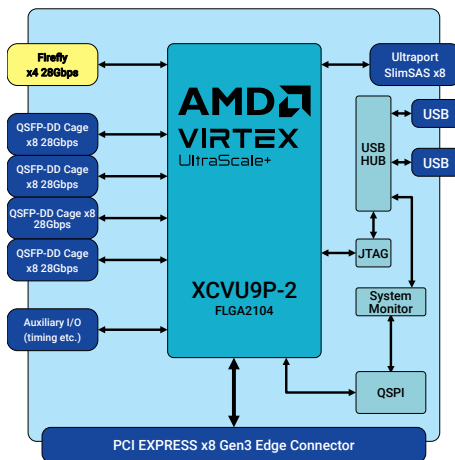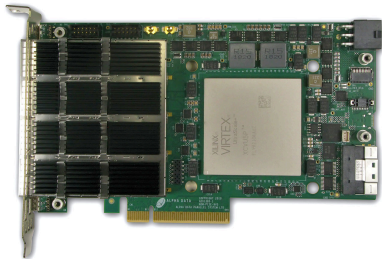AD01385

Applications

- Low Latency Trading
- In-Network Compute
- High-Frequency Trading
- High-speed Communications Hub

Board Features

- x8 Gen3 PCIE
- 4x QSFP-DD Cages
- 1x OpenCAPI Interface
- 1x Firefly Interface (optional)
- 1x PPS synchronisation Input

Summary

The ADM-PCIE-9V5 is a single-slot, half-length, full-height PCI Express Add-In Card featuring the powerful and efficient AMD Virtex UltraScale Plus VU9P-3 FPGA.

It offers an 8-lane PCIe Gen3 capable interface and front IO with 4x QSFP-DD sockets, each supporting either two 100GbE or eight 10/25GbE interfaces. Additionally, it includes an onboard Ultraport SlimSAS Connector for OpenCAPI Connectivity.

System monitoring of temperature, voltage, and current provides developers with accurate feedback on power utilization for their designs.

Block Diagram

- Firefly x4 28Gbps
- Ultraport SlimSAS x8
- USB
- USB HUB
- USB
- QSFP-DD Cage x8 28Gbps
- QSFP-DD Cage x8 28Gbps
- QSFP-DD Cage x8 28Gbps
- QSFP-DD Cage x8 28Gbps
- AMD VIRTEX UltraScale+ XCVU9P-2 FLGA2104
- JTAG
- System Monitor
- Auxiliary I/O (timing etc.)
- QSPI
- PCI EXPRESS x8 Gen3 Edge Connector

Target Devices

AMD Virtex UltraScale Plus
XCVU9P-3, XCVU5P-3 (FLGA2104/FLVA2104)

LUTs = 1182k FFs = 2364k
DSPs = 6840
BRAM = 75.9Mb(36Mb) URAM = 270.0Mb (132.2Mb)

9x 100G Ethernet MACs (incl. KR4 RS-FEC) (6 on VU5P-3)
9x 150G Interlaken cores (6 on VU5P-3)
6x PCI Express x16 Gen3 cores (4 on VU5P-3)

FPGA Notes

For the FPGA packages used for this product, certain GTY tiles are unavailable because they are not bonded to physical pins. This means that, in order to make use of certain hard CMAC, PCIe and Interlaken cores, the 'Pipe' scheme must be used, in which the core in question is routed to bonded GTY tile(s) using pipelining registers. For diagrams showing bonded and unbonded GTY tiles, please refer to Figures 1-90 (VU5P in FLV2104 package) and 1-99 (VU9P in FLGA2104 package) in : https://www.xilinx.com/support/documentation/user_guides/ug575-ultrascale-pkg-pinout.pdf (v1.13)

Configuration Memory

QSPI 2GBit Flash Memory

Configuration Modes

From onboard Flash
Through USB board management (built-in JTAG)
Partial Reconfiguration (via MCAP) Over PCIE

Deliverables

ADM-PCIE-9V5 Board
One Year Warranty
One Year Technical Support

Host Interface

PCI Express Gen3 x8 or OpenCAPI

Communications Interfaces

4x QSFP-DD 8x28Gbps - User Configurable, includes 10/25/40/100G Ethernet

1x Ultraport SlimSAS 8x25Gbps - OpenCAPI

1x Firefly 4x28Gbps - User Configurable

Input/Output Interfaces

Other Interfaces

USB (front and rear sockets) board management (built-in JTAG)

Isolated PPS Timing Input

Board Management

The ADM-PCIE-9V5 houses a system monitoring chip which can provide real-time temperature, voltage and current readings of the system, as well as reconfigure programmable clocks and much more. The system monitor can be accessed directly through the USB interface via the front panel (or rear of the board), the UART connection to the target FPGA or through the SMBus interface on the card's PCI Express edge connector. When enabled**, IPMI can also be used to communicate with the system monitor, allowing for remote communication and management with the ADM-PCIE-9V5.
** IPMI is disabled by default and should only be enabled when the board is installed in an IPMI-compliant system. Please contact the factory for details on enabling IPMI on the ADM-PCIE-9V5.

Support

TBC

Board Format

Single Slot 1/2 Length, Full Height, x8 PCIe form Factor
WxHxD = 181.5mm x 120.9mm x 19.7mm
Weight = Without Fan - 590g

Environmental Specification

Cooling Option	Operating Temperatures		Storage Temperatures	
	Min	Max	Min	Max
AC0	0°C	+55°C	-40°C	+85°C

Operating Humidity : Up to 95% (non-condensing)

EMC Standards

See the ADM-PCIE-9V5 Declaration of Conformity document

Ordering Information
Order Code: ADM-PCIE-9V5(x)

Option	Code	Description of Options
FPGA Select	x	blank=Standard COTS product with XCVU9P-3, /VU5P-3='standard' variant with XCVU5P-3
Note		Other options are available, please contact sales for details.