# ADM-XRC-4 (LX/SX)

PCI Mezzanine Card

User Guide

Version 1.4

Alpha Data
4 West Silvermills Lane
Edinburgh EH3 5BD
UK

Phone: +44 (0) 131 558 2600
Fax: +44 (0) 131 558 2700
Email: support@alphadata.co.uk

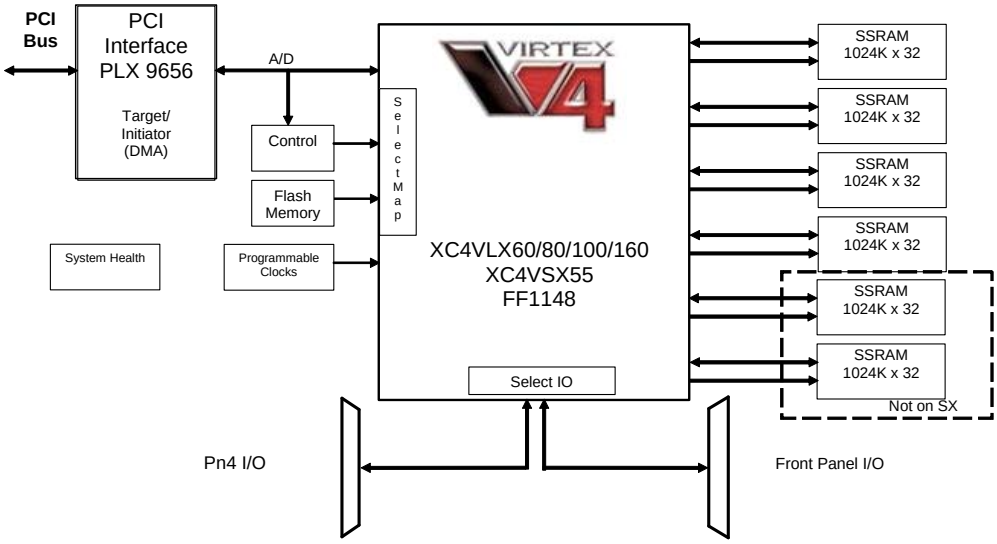
Alpha Data
2570 North First Street, Suite 440
San Jose, CA 95131
USA

Phone: (408) 467 5076
Fax: (866) 820 9956
Email: support@alpha-data.com

Table of Contents

# 1. Introduction

The ADM-XRC-4 (LX/SX) is a high performance PCI Mezzanine Card (PMC) format device designed for supporting development of applications using the Virtex-4 series of FPGA's from Xilinx.




## 1.1. Specifications

The ADM-XRC-4 (LX/SX) supports high performance PCI operation without the need to integrate proprietary cores into the FPGA. A PLX PCI9656 provides a rich set of PCI resources including two high-speed DMA.

- Physically conformant to IEEE P1386-2001 Common Mezzanine Card standard
- High performance PCI and DMA controllers
- Local bus speeds of up to 66MHz
- Six banks (four on SX) of 256k/512k/1024Kx32 ZBT SSRAM
- User clock programmable between 20MHz and 500MHz
- Stable low-jitter 200MHz clock for precision IO delays
- User front panel adapter with up to 146 free IO signals
- User rear panel PMC connector with 64 free IO signals
- Programmable 2.5V or 3.3V I/O on front and rear interfaces
- Supports 3.3V and 5V PCI signalling levels (VI/O)
- LX Version supports XC4VLX80, 100 and 160
- SX version supports SX55

# 2. Installation

This chapter explains how to install the ADM-XRC-4 (LX/SX) onto a PMC motherboard.

## 2.1. Motherboard requirements

The ADM-XRC-ADM-XRC-4 is a Universal PCI device and supports both 3.3V and 5V PCI signalling levels (VI/O).
The ADM-XRC-ADM-XRC-4 must be installed in a PMC motherboard that supplies 3.3V power to the PMC connectors. Ensure that the motherboard satisfies this requirement before powering it up.

## 2.2. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

## 2.3. Installing the ADM-XRC-ADM-XRC-4 onto a PMC motherboard

**Note: This operation should not be performed while the PMC motherboard is powered up.**
The ADM-XRC-4 (LX/SX) must be secured to the PMC motherboard using M2.5 screws in the four holes provided. The PMC bezel through which the I/O connector protrudes should be flush with the front panel of the PMC motherboard.

## 2.4. Installing the ADM-XRC-ADM-XRC-4 if fitted to an ADC-PMC

The ADM-XRC-4 (LX/SX) can be supplied for use in standard PC systems fitted to an ADC-PMC carrier board. The ADC-PMC can support up to two ADC-PMC cards whilst maintaining host PC PCI compatibility. If you are using a ADC-PMC refer to the supplied documentation for information on jumper settings. All that is required for installation is a PCI slot that has enough space to accommodate the full-length card. The ADC-PMC is compatible with 5V and 3V PCI (32 and 64 bit) and PCI-X slots.

It should be noted that the ADC-PMC uses a standard bridge to provide a secondary PCI bus for the ADM-XRC-4 (LX/SX) and that some older BIOS code does not set up these devices correctly. Please ensure you have the latest version of BIOS appropriate for your machine.

# 3. Software Installation

Please refer to the SDK installation CD for Windows. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing. For users of the ADM-XRC-II, the ADM-XRC-4 is very similar and interfacing techniques are the same. The main difference between the two boards from a user perspective is in the UCF information supplied in the SDK.

# 4. Board Overview

The ADM-XRC-4 (LX/SX) is a high performance PMC aimed at embedded I/O applications where flexibility, ease of use and re-configurability are paramount.

The ADM-XRC-4 has been designed as a successor to the ADM-XRC-II and offers a simple upgrade path to Virtex™-4 technologies. Existing applications can be ported very easily with the minimum of change.

With 6/4 banks of ZBT memory, each with its own clock domain, designs can be optimised more easily where multiple clocks exist.

## 4.1. PCI and Bridging

The ADM-XRC-4 uses an off-the-shelf bridge solution from PLX Technology, the PCI9656. This device supports 64/32 bit and 66/33MHz PCI interfaces with universal signalling. An EEPROM contains initialisation data for the bridge and also some information relating to ADM-XRC-4 resources such as serial number, memory capability and FPGA type.

The bridge implements DMA with two controllers for high performance data transfer. It also permits the User FPGA to initiate and control transfers on the PCI bus anywhere in 32 bit space.

## 4.2. Local Bus

The local bus on the ADM-XRC-4 is always 32 bits wide and supports bus speeds up to 66MHz, asynchronous from PCI speed. A range of transfer mechanisms are supported with either the PCI Bridge or User FPGA initiating data movement.

## 4.3. User FPGA and Memory

The User FPGA is a Virtex™-4 device selected from the LX or SX ranges. Both cards support the FF1148 package to provide a wide range of device options. The SX version of the board is designed to maximise I/O compatibility with the LX version and other XRC series cards. It achieves this by sacrificing memory capacity due to the reduced overall I/O count of the SX55 device.

Compatibility between LX and SX exists on all I/O except for the front panel I/O. Therefore local bus, Pn4 and 4 bank memory applications are completely source code and UCF compatible.

## 4.4. Control Logic and Flash

The ADM-XRC-4 has improved control logic compared to the ADM-XRC-II. In addition to managing User FPGA configuration and interrupts, support for host JTAG access, temperature monitoring and XRM identification are provided. The control logic is implemented in a Spartan-3 device and options will be provided for users to access embedded local bus Chipscope Pro analysers to monitor the behaviour of designs.

The control logic manages the attached flash for storing User FPGA bit-streams intended for configuration on cold-boot.

### 4.5. Clocks

The ADM-XRC-4 has enhanced clocking capabilities compared to earlier XRC series cards. The ability to control LCLK up to 66MHz is still available. In addition, a programmable frequency low-jitter LVPECL MCLK is provided capable of 20 to 500MHz performance.

To support the IDELAY feature of Virtex™-4 devices, a dedicated 200MHz LVPECL oscillator is fitted as standard to all ADM-XRC-4 variants. If required, this clock may be used for any purpose the user requires.

### 4.6. Pn4 I/O

A full differential signalling implementation is provided on Pn4. The 32 pairs of signals are all routed with 100 Ohm impedance and wire directly to the User FPGA.

The VCCO (IO voltage) of the User FPGA bank connected to Pn4 differential pairs can be selected by host software for 2.5V or 3.3V levels.

### 4.7. XRM Bus

The ADM-XRC-4 supports the XRM bus to enable the use of I/O adaptors to cater for many potential interface problems. Many XRM's have been developed by Alpha Data and its partners to provide a wide range of interfacing solutions. The ability to design XRM's for situations where no standard product exists is often a cost-effective route for customers.

Up to 68 differential clock pairs plus 4 bidirectional clock pairs are available.

The VCCO (IO voltage) of the User FPGA bank connected to the XRM bus can be selected by jumper for 2.5V or 3.3V levels.

### 4.8. Health Monitoring

In order to check the integrity of the card during normal operation the 1.2V, 2.5V, 3.3V and 5V supplies along with the board and User FPGA temperatures are monitored by an on-board device. The measurements can be easily accessed from the host.

# 5. PCI Bridge

The PCI bus is implemented in a PLX PCI9656 and is configured with settings as described later in this document to simplify the integration of user applications in the FPGA.

The PCI9656 uses the first two Bar's to provide access to its internal registers both via memory accesses and I/O accesses. Either BAR may be used by the host.

BAR 2 provides access to a 4Mbyte space for use by the FPGA and must be accessed only when a valid FPGA configuration is loaded that can respond correctly to local bus access.

BAR 3 provides access to the local control registers and the flash memory.

The ADM-XRC-4 is identified firstly as PLX bridge device by the device/vendor ID (0x10B5/0x9656) and then through the sub-vendor and device ID values as shown in the table below.

| Card | Sub-System Vendor ID | Sub-System Device ID |
|---|---|---|
| ADM-XRC-4LX | 0x4144 | 0x004C |
| ADM-XRC-4SX | 0x4144 | 0x004D |

**Table 1 PCI Device Identification**

The Alpha Data driver uses these values to determine exactly what type of card is fitted.

The PCI configuration space of the ADM-XRC-ADM-XRC-4 is shown below.

| Config. Offset | 31 24 | 23 16 | 15 8 | 7 0 |
|---|---|---|---|---|
| 00 | Device ID (9656) | | Vendor ID (10B5) | |
| 04 | Status | | Command | |
| 08 | Class Code | | | RevisionID |
| 0C | BIST | HeaderType | Lat. Timer | Cache Line |
| 10 | PCI BAR0 (PLX Internal Registers/Memory) | | | |
| 14 | PCI BAR1 (PLX Internal Registers/IO) | | | |
| 18 | PCI BAR2 (Local Bus FPGA) | | | |
| 1C | PCI BAR3 (Local Bus Control/Flash/SelectMap) | | | |
| 20 | PCI BAR4 (Not used) | | | |
| 24 | PCI BAR5 (Not used) | | | |
| 28 | Card Bus CIS Pointer(Not used) | | | |
| 2C | See Table | | 4144 | |
| 30 | PCI Base Address for Local Expansion ROM | | | |
| 34 | Reserved | | | |
| 38 | Reserved | | | |
| 3C | Max Lat | Min Gnt | Int. Pin | Int. Line |

**Table 2 PCI Configuration Space**

# 6. Local Bus

The Local Bus is the interconnection between the PCI Bus Bridge (PLX 9656) and the User FPGA. The bus uses PLX 9656 C Mode protocol to provide an interface with separate address and data busses, control signals and clocks. Data transfers between the host system and the FPGA flow across the bus using a simple protocol based on burst transfers using start and end control signals.

The bus supports DMA transfers for maximum performance with local bus clock speeds of up to 66MHz. A very useful feature of the DMA unit of the PLX is demand-mode transfer. This mode allows the FPGA to trigger each transfer of the DMA in single or burst cycles to throttle the throughput depending on processing needs. Such situations exist where FIFO's are used and empty or full conditions need to be considered and data is not always available.

The diagram below shows the mapping of PCI bus space to Local Bus via the PLX9656. The user should not access the Local Bus control registers because these are controlled by the ADM-XRC series software driver. It is possible to access these with care, see Section 8 of this manual.

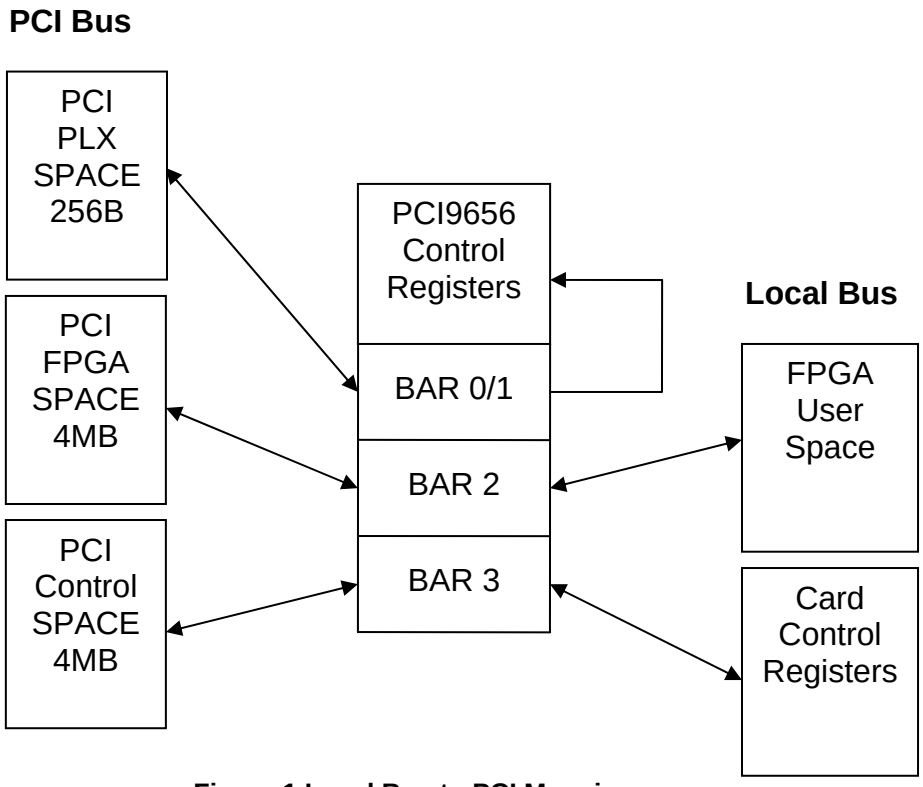



**Figure 1 Local Bus to PCI Mapping**

There are examples in the SDK demonstrating the use of the local bus and more information in the SDK help files.

## 6.1. Characteristics of Address Spaces

The ADM-XRC-4 maps two PCI BAR spaces to the local bus and are specified to operate as shown below.

| Space | Size | Width | Burst | Prefetch | Burst Term | Local Offset |
|---|---|---|---|---|---|---|
| S0 | 4MB | 32 | yes | no | yes | 0x00000000 |
| S1 | 4MB | 32 | yes | no | yes | 0x80000000 |

**Table 3 Local Bus Address Space**

From the PCI side of the PCI9656, transfers to either space may be 8, 16 or 32-bit in width and of any length. The PCI9656 breaks up transfers to suit the address space on the local bus whilst respecting the characteristics outlined above.

It should be noted that the Control Logic implemented on the local bus by a Spartan-3 device decodes all of S1 when accessed by the PLX bridge. This region is then sub-divided into burst and non-burst segments depending on the functional area accessed.

# 7. User FPGA

The User FPGA is the main focus of the ADM-XRC-4 in terms of capability and performance. The Virtex™-4 FPGA series from Xilinx is the latest family of application-domain-optimised devices especially suited for high speed advanced re-configurable uses in embedded systems, IP development and co-processing applications.

The 4LX is designed primarily to support the LX range of parts from LX80 to LX160 in FF1148 packages. Intended for mainly logic applications, these devices feature up to 288 BRAM's, 96 XtremeDSP slices and 12 DCM's.

The 4SX is designed to support the SX55 but with only 4 banks of SRAM. This reduction in capability is offset by the maintenance of all other features – a benefit of the new banking arrangement of Virtex™-4.

## 7.1. Configuration

The ADM-XRC-4 performs configuration from the host at high speed using SelectMAP. The FPGA may also be configured from flash or by JTAG via header J5.

Download from the host is the fastest way to configure the User FPGA with 8 bit SelectMAP mode enabled. This permits an ideal configuration speed of up to 66MB/s.

The ADM-XRC-4 can be configured to boot the User FPGA from flash on power up if a valid bit-stream is detected in the flash. Booting from flash will also configure the clocks and I/O voltages as appropriate.

**NOTE**. Boards supplied with Engineering Silicon (ES) devices will already have a bitstream in flash and this will be loaded on power up of the card. This default bitstream performs no I/O function but simply maintains data sheet requirements for configuration with 10 minutes of power up, see parameter $T_{CONFIG}$ in the Xilinx data sheet. This is essential if data sheet parameters for DCM operation are to be met.

## 7.2. I/O Bank Voltages

The Virtex-4 series of devices in FF1148 packages fitted to the ADM-XRC-4 are configured with up to 15/13 banks of I/O pins.

| Banks | Power Supply | Comment | Board Specific |
|---|---|---|---|
| 9, 11, 13 | 2.5 or 3.3 | Front Panel I/O | 4LX |
| 7, 9, 11 | 2.5 or 3.3 | Front Panel I/O | 4SX |
| 1, 2, 3, 4 | 3.3 | Local Bus | |
| 12 | 2.5 or 3.3 | Pn4 I/O (3.3 default) | |
| 0 | 2.5 | VCCAUX Configuration | |
| 5, 6, 8, 10 | 2.5 | SRAM Banks | |
| 7, 14 | 2.5 | SRAM Banks | 4LX |

**Table 4 FPGA I/O Bank Voltages**

The main difference between the 4LX and 4SX is with front panel I/O and SRAM banks and is because the SX55 device does not have I/O banks 13 and 14.

### 7.3. Memory Interfaces

There are up to six or four interfaces on the ADM-XRC-4 respectively, each of which supports up to 1024Kx32 of ZBT, also known as No Bus Turnaround memory. Each interface is allocated to a User FPGA bank and is independently clocked.

Each memory interface supports the following signals.

| Signal | Bus | Active | Typical UCF signal | FPGA In/Out |
|---|---|---|---|---|
| Address | [20:0] | High | rax<20:0> | O |
| Data | [31:0] | High | rdx<31:0> | I/O |
| Byte enables | [3:0] | Low | rcx<3:0> | O |
| Write | | High | rcx<4> | O |
| Output enable | | Low | rcx<7> | O |
| Advance/Load | | High | rcx<6> | O |
| Chip enable | | Low | rcx<5> | O |
| Clock | | High | ramclko<x> | O |
| Clock feedback | | High | ramclki<x> | I |

The UCF signal names are taken from the example files provided in SDK 4.7.0. Replace “x” in the signal name with the bank number to match the signals in each memory bank.

The standard memory device fitted is a Samsung K7N323645M-FC16. This is a 2.5V core, 2.5V I/O device with a maximum operating frequency of 166MHz.

It should be noted that device signal CKE_L, clock enable, is tied low and permanently enabled. The LBO_L signal is similarly tied low to enable linear burst. Although there are three chip enables on the ZBT device only CE_L is programmable by the FPGA. The other two chip enables on the device are tied active on the PCB.

All ZBT memory interfaces use 2.5V power I/O supplies. Virtex-4 I/O standards should be selected using this power source only, e.g. LVCMOS25.

See Section 9 for information on how the clocks are routed and fed-back for DCM de-skew.

# 8. Control Logic and Flash

The ADM-XRC-4 uses a Spartan-3 XC3S200, referred to as S3, device to manage access to resources on the card such as configuration ports, health monitoring, clocks, interrupts (from the FPGA) and flash memory. The S3 is booted automatically on power up from a serial configuration device.

The description of registers and functionality of the S3 is currently the subject of a separate manual and will be incorporated in a future version of this document.

## 8.1. Flash Interface

The ADM-XRC-4 is fitted with an Intel RC28F128J3C flash device and it is used for storing bitstream data. During power up, and after the S3 is configured, the control logic checks for a valid bitstream in flash and if present proceeds to load it into the FPGA. The process of loading the FPGA from flash can be inhibited by setting a jumper on the JTAG connector. See Section 13 for further information.

Access to the flash device is only possible through S3 registers. The flash is not directly mapped onto the local bus.

Programming, erasing and verification of the flash is supported by the ADM-XRC SDK and driver. Utilities are provided to load bitstreams into the flash. These also verify the bitstream is compatible with the target FPGA.

# 9. Clocks

The ADM-XRC-4 is provided with numerous clock sources of much higher quality than in previous generations of XRC PMC.

## 9.1. LCLK

The Local Bus can be used at up to 66MHz and all timing is synchronised to LCLK between the PLX bridge, User FPGA and Control Logic. LCLK is generated by an ICS307 synthesiser using a base 25MHz crystal.

## 9.2. MCLK

The User FPGA has a single dedicated clock MCLK that is generated by an ICS8430-61 LVPECL synthesiser. This device has two outputs of the same clock, one of which is routed to the User FPGA whilst the other is routed to the XRM connector. Both are terminated using LVPECL terminations.

MCLK can be programmed between 20MHz and 500MHz. The ICS8430 has its own 25MHz crystal for generating the reference clock for the synthesiser.

## 9.3. REFCLK

In order to make use of the IDELAY feature of Virtex™-4, a stable low-jitter clock source is required to provide the base timing for tap delay lines in each IOB in the User FPGA. The ADM-XRC-4 is fitted with a 200MHz LVDS (LVPECL optional) oscillator module connected to global clock resource pins. This reference clock can also be used for application logic if required.

## 9.4. SRAM Clocks

There are 6 banks of SRAM, each of which has its own clock output sourced from the User FPGA bank that connects to each SRAM device. Each clock also has a feedback path to global clock resource pins for de-skew if required by the user.

It should be noted that all SRAM banks use 2.5V signalling but the global clock feedback pins are connected on central resource pins powered from 3.3V. These feedback pins have 100R in series to protect the 2.5V bank signals from inadvertent back driving from rogue bit-streams.

| RAM Bank | LX Clock pin | SX Clock Pin | Feedback LX/SX |
|---|---|---|---|
| 0 | R9 | R9 | AE17 |
| 1 | J7 | J7 | AG18 |
| 2 | F31 | F31 | G17 |
| 3 | AN9 | AN9 | AH19 |
| 4 | AM25 | Not fitted | K19 |
| 5 | W10 | Not fitted | AK18 |

**Table 5 SRAM Clocks and Feedback**

## 10. Pn4 I/O

Up to 32 pairs of differential or 64 single-ended signals are available on Pn4 and all are sourced from Bank 12 of the User FPGA. All of the signal traces are routed as 100 Ohm differential pairs and each pair is matched in length. The worst case difference in trace length between any two pairs is 5mm.

User FPGA Bank12/Pn4 can use 3.3V or 2.5V signalling standards selectable through the control logic. The default power state for Bank 12 is configured by the control logic to be 3.3V but can be changed under software control.

| Signal | FPGA Pin | Pn4 Pin | Pn4 Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| PN4_P1 | AB6 | 1 | 2 | AB5 | PN4_N1 |
| PN4_P2 | AC3 | 3 | 4 | AC2 | PN4_N2 |
| PN4_P3 | Y11 | 5 | 6 | AA11 | PN4_N3 |
| PN4_P4 | AD2 | 7 | 8 | AD1 | PN4_N4 |
| PN4_P5 | Y14 | 9 | 10 | AA13 | PN4_N5 |
| PN4_P6 | AC5 | 11 | 12 | AC4 | PN4_N6 |
| PN4_P7 | AF1 | 13 | 14 | AE1 | PN4_N7 |
| PN4_P8 | AA9 [CC] | 15 | 16 | AA8 [CC] | PN4_N8 |
| PN4_P9 | Y13 [CC] | 17 | 18 | Y12 [CC] | PN4_N9 |
| PN4_P10 | AE3 | 19 | 20 | AE2 | PN4_N10 |
| PN4_P11 | AD6 | 21 | 22 | AD5 | PN4_N11 |
| PN4_P12 | AC7 | 23 | 24 | AB8 | PN4_N12 |
| PN4_P13 | Y16 | 25 | 26 | AA15 | PN4_N13 |
| PN4_P14 | AE4 | 27 | 28 | AD4 | PN4_N14 |
| PN4_P15 | AH3 | 29 | 30 | AH2 | PN4_N15 |
| PN4_P16 | AG2 | 31 | 32 | AG1 | PN4_N16 |
| PN4_P17 | AC9 | 33 | 34 | AC8 | PN4_N17 |
| PN4_P18 | AG3 | 35 | 36 | AF3 | PN4_N18 |
| PN4_P19 | AF6 | 37 | 38 | AE6 | PN4_N19 |
| PN4_P20 | AF5 | 39 | 40 | AF4 | PN4_N20 |
| PN4_P21 | AL1 | 41 | 42 | AK1 | PN4_N21 |
| PN4_P22 | AJ2 | 43 | 44 | AJ1 | PN4_N22 |
| PN4_P23 | AG6 [*] | 45 | 46 | AG5 [*] | PN4_N23 |
| PN4_P24 | AE7 [CC] | 47 | 48 | AD7 [CC] | PN4_N24 |
| PN4_P25 | AC10 [CC] | 49 | 50 | AB10 [CC] | PN4_N25 |
| PN4_P26 | AK3 | 51 | 52 | AK2 | PN4_N26 |
| PN4_P27 | AF8 | 53 | 54 | AE8 | PN4_N27 |
| PN4_P28 | AH5 | 55 | 56 | AH4 | PN4_N28 |
| PN4_P29 | AB13 | 57 | 58 | AB12 | PN4_N29 |
| PN4_P30 | AM2 | 59 | 60 | AM1 | PN4_N30 |
| PN4_P31 | AG8 | 61 | 62 | AG7 | PN4_N31 |
| PN4_P32 | AM3 | 63 | 64 | AL3 | PN4_N32 |

**Table 6 Pn4 to FPGA Assignments**

Pins marked [CC] are clock capable I/O and cannot be used as differential outputs.

Pins marked [*] are dual purpose. These are also DCI pins and can be strapped to provide controlled impedance but are then unusable as I/O. The diagram in Figure 2 Pn4 DCI Resistor Configuration illustrates how DCI can be configured. Fitting R2/R3 permits the use of Pn4_P23/N23 as I/O and R4/R5 must not be fitted. Fitting R4/R5 and removing R2/R3 allows DCI functionality to be invoked for Bank 12 for I/O pins that need it.

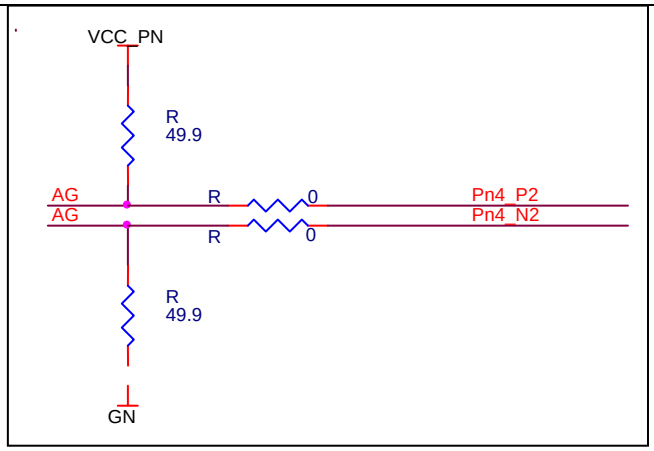



**Figure 2 Pn4 DCI Resistor Configurations**

By default, all cards are supplied with R2/R3 fitted and R4/R5 omitted. This allows signal pair 23 to be used for Pn4 I/O.

## 10.1. Pn4 Power Supply Control

The power supply for the FPGA bank containing the I/O pins for Pn4 is by default configured for 3.3V operation. With control logic firmware revision 1.4 it is not possible to change this setting.

With version 1.5 firmware and later, it is possible to change VCC_PN4 under software control.

Within the control logic address space on the local bus there are registers to control various resources. In particular, the PWRCTL register at offset 0x28 can be used to change the Pn4 power supply. To avoid unintended changes to the power supply setting a sequence of write operations to PWRCNTL must be used to effect a change.

The sequence is 0x00000055, 0x000000AA followed by 0x0000_000y where y=3 for 3.3V and y=2 for 2.5V. Writing y=0 will turn off Pn4 power.

# 11. XRM Bus and Front Panel I/O

A major benefit of the ADM-XRC series of boards that use the XRM Bus interface is the versatility of I/O options that result. The ADM-XRC-4 maintains this interface and thus compatibility with a wide range of I/O modules to suit many diverse needs.

The XRM interface uses the Samtec QSH series 180 pin connector for all signalling and power.

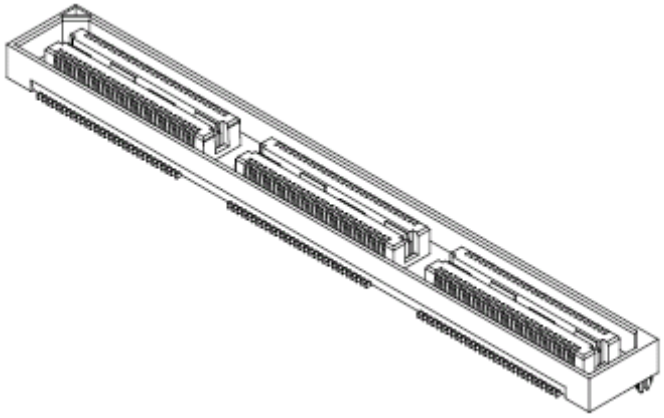


**Figure 3 XRM Connector - Samtec QSH**

A full list of the signal interface for the XRM interface implemented on both LX and SX boards follows.

## 11.1. XRM Signalling Voltage

The signalling voltage on the XRM connector is determined by jumper J7. Linking pins 1 and 2 will select 3.3V for VCCIO. Removing the jumper and parking it on pin 4 selects 2.5V.

It should be noted that J7 does not directly route power to the XRM. The link position is monitored by the Spartan 3 control logic which in turn sets the power multiplexer for the XRM to be 2.5V or 3.3V.

## 11.2. XRM Interface – LX Version

The XRM interface is implemented on CN1, a 180 pin Samtec connector type QSH, with the pin-out as detailed in the tables that follow in Table 7 to Table 9.

In turn, the signals that connect to CN1 are provided in the main from three banks of the User FPGA, Banks 9, 11 and 13. These banks share a common VCCO that can be 2.5V or 3.3V powered, selectable under user control.

| Signal | FPGA Pin | Samtec Pin | Samtec Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| N_1 | H28 | 1 | 2 | D32 | N_2 |
| P_1 | H27 | 3 | 4 | C32 | P_2 |
| N_3 | K27 | 5 | 6 | N22 | P_4 |
| P_3 | J27 | 7 | 8 | N23 | N_4 |
| N_5 | H30 | 9 | 10 | J30 | N_6 |
| P_5 | H29 | 11 | 12 | J29 | P_6 |
| N_7 | E33 | 13 | 14 | R21 | N_8 |
| P_7 | E32 | 15 | 16 | P22 | P_8 |
| P_9 | C33 | 17 | 18 | K28 | P_10 |
| N_9 | C34 | 19 | 20 | K29 | N_10 |
| N_11 | G33 | 21 | 22 | L31 | N_12 (cc) |
| P_11 | G32 | 23 | 24 | L30 | P_12 (cc) |
| N_13 | L34 | 25 | 26 | M32 | P_14 |
| P_13 | L33 | 27 | 28 | M33 | N_14 |
| N_15 | R19 | 29 | 30 | L28 | P_16 |
| P_15 | P20 | 31 | 32 | L29 | N_16 |
| N_17 | R24 | 33 | 34 | M28 | N_18 |
| P_17 | P24 | 35 | 36 | M27 | P_18 |
| S_1 | G31 | 37 | 38 | D34/F33 | CLK0_P |
| +3V3 | | 39 | 40 | E34/F34 | CLK1_N |
| +3V3 | | 41 | 42 | | XRM_SERID |
| +3V3 | | 43 | 44 | | RESERVED |
| +5V | | 45 | 46 | | XRM_VREF |
| +5V | | 47 | 48 | | XRM_VCCIO |
| XRM_VBAT | | 49 | 50 | | XRM_VCCIO |
| +12V | | 51 | 52 | | XRM_VCCIO |
| +12V | | 53 | 54 | | -12V |
| PRESENCE | | 55 | 56 | | XRM_TDI |
| XRM_TCK | | 57 | 58 | | XRM_TRST |
| XRM_TMS | | 59 | 60 | | XRM_TDO |

**Table 7 LX XRM Bus Interface Part 1**

| Signal | FPGA Pin | Samtec Pin | Samtec Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| N_19 | H34 | 61 | 62 | K33 | N_20 |
| P_19 | H33 | 63 | 64 | K32 | P_20 |
| N_21 | P27 | 65 | 66 | K34 | N_22 |
| P_21 | N27 | 67 | 68 | J34 | P_22 |
| N_23 | N30 | 69 | 70 | V30 | N_24 (cc) |
| P_23 | N29 | 71 | 72 | W30 | P_24 (cc) |
| N_25 (cc) | Y33 | 73 | 74 | T23 | P_26 |
| P_25 (cc) | Y32 | 75 | 76 | U23 | N_26 |
| P_27 | R26 | 77 | 78 | T25 | N_28 |
| N_27 | T26 | 79 | 80 | T24 | P_28 |
| N_29 | R29 | 81 | 82 | N32 | P_30 |
| P_29 | P29 | 83 | 84 | P32 | N_30 |
| N_31 | P31 | 85 | 86 | T31 | N_32 |
| P_31 | P30 | 87 | 88 | R31 | P_32 |
| CLK2_P | P34/R32 | 89 | 90 | V34 | N_33 |
| CLK3_N | R34/R33 | 91 | 92 | V33 | P_33 |
| N_34 | T34 | 93 | 94 | U27 | N_35 |
| P_34 | T33 | 95 | 96 | U26 | P_35 |
| CLK4_P | AF29/AG30 | 97 | 98 | U31 | N_36 |
| CLK5_N | AF30/AG31 | 99 | 100 | U30 | P_36 |
| N_37 | U33 | 101 | 102 | AA25/AC28 | CLK6_P |
| P_37 | U32 | 103 | 104 | AA26/AB28 | CLK7_N |
| N_38 | U25 | 105 | 106 | H32 | S_2 |
| P_38 | V25 | 107 | 108 | | RESERVED |
| RESERVED | | 109 | 110 | | RESERVED |
| RESERVED | | 111 | 112 | | RESERVED |
| MCLK_N | | 113 | 114 | | RESERVED |
| MCLK_P | | 115 | 116 | | RESERVED |
| RESERVED | | 117 | 118 | | RESERVED |
| RESERVED | | 119 | 120 | | RESERVED |

**Table 8 LX XRM Bus Interface Part 2**

| Signal | FPGA Pin | Samtec Pin | Samtec Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| P_39 | V23 | 121 | 122 | W32 | P_40 |
| N_39 | V24 | 123 | 124 | V32 | N_40 |
| N_41 | V27 | 125 | 126 | Y29 | P_42 |
| P_41 | W27 | 127 | 128 | W29 | N_42 |
| P_43 | AB32 | 129 | 130 | AA33 | P_44 |
| N_43 | AB33 | 131 | 132 | AA34 | N_44 |
| N_45 | AA31 | 133 | 134 | Y28 | N_46 |
| P_45 | AB31 | 135 | 136 | Y27 | P_46 |
| P_47 | T29 | 137 | 138 | AH34 | N_48 |
| N_47 | T30 | 139 | 140 | AJ34 | P_48 |
| P_49 | AA23 | 141 | 142 | AA29 | N_50 |
| N_49 | AA24 | 143 | 144 | AA28 | P_50 |
| N_51 | AE34 | 145 | 146 | AB30 | P_52 |
| P_51 | AE33 | 147 | 148 | AA30 | N_52 |
| P_53 | AG32 | 149 | 150 | AC30 | N_54 |
| N_53 | AG33 | 151 | 152 | AC29 | P_54 |
| P_55 | AD27 | 153 | 154 | Y24 | N_56 |
| N_55 | AC27 | 155 | 156 | W24 | P_56 |
| N_57 | AD29 | 157 | 158 | AD32 | N_58 |
| P_57 | AE29 | 159 | 160 | AE32 | P_58 |
| P_59 | AC32 | 161 | 162 | AE31 | N_60 |
| N_59 | AC33 | 163 | 164 | AF31 | P_60 |
| N_61 | AL34 | 165 | 166 | AF34 | N_62 |
| P_61 | AL33 | 167 | 168 | AF33 | P_62 |
| N_63 | AH33 | 169 | 170 | AB23 | N_64 |
| P_63 | AH32 | 171 | 172 | AB22 | P_64 |
| N_65 | AM33 | 173 | 174 | AK34 | N_66 |
| P_65 | AM32 | 175 | 176 | AK33 | P_66 |
| N_67 | AH30 | 177 | 178 | AL31 | N_68 |
| P_67 | AJ30 | 179 | 180 | AM31 | P_68 |

**Table 9 LX XRM Bus Interface Part 3**

Signals marked P_x/N_x and CLKn_P/CLKn+1_N are differential pairs routed for 100R impedance under differential conditions. These can be used single ended if required.
Signals marked S_y are single ended and routed with 50R impedance.

MCLK_P/N is an LVPECL copy of the ADM-XRC-4 MCLK user clock signal. It is terminated on the ADM-XRC-4L.

Signals marked with XRM_ are housekeeping signals and are not user programmable.

### 11.3. XRM Interface – SX Version

The XRM interface is implemented on CN1, a 180 pin Samtec connector type QSH, with the pin-out as detailed in the tables that follow in Table 10 to Table 12.

In turn, the signals that connect to CN1 are provided from three banks of the User FPGA - Banks 9, 11 and 13. These banks share a common VCCO that can be 2.5V or 3.3V powered, selectable under user control.

| Signal | FPGA Pin | Samtec Pin | Samtec Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| N_1 | H28 | 1 | 2 | D32 | N_2 |
| P_1 | H27 | 3 | 4 | C32 | P_2 |
| N_3 | K27 | 5 | 6 | N22 | P_4 |
| P_3 | J27 | 7 | 8 | N23 | N_4 |
| N_5 | H30 | 9 | 10 | J30 | N_6 |
| P_5 | H29 | 11 | 12 | J29 | P_6 |
| N_7 | E33 | 13 | 14 | R21 | N_8 |
| P_7 | E32 | 15 | 16 | P22 | P_8 |
| P_9 | C33 | 17 | 18 | K28 | P_10 |
| N_9 | C34 | 19 | 20 | K29 | N_10 |
| N_11 | G33 | 21 | 22 | L31 | N_12 |
| P_11 | G32 | 23 | 24 | L30 | P_12 |
| N_13 | L34 | 25 | 26 | M32 | P_14 |
| P_13 | L33 | 27 | 28 | M33 | N_14 |
| N_15 | R19 | 29 | 30 | L28 | P_16 |
| P_15 | P20 | 31 | 32 | L29 | N_16 |
| N_17 | R24 | 33 | 34 | M28 | N_18 |
| P_17 | P24 | 35 | 36 | M27 | P_18 |
| S_1 | G31 | 37 | 38 | F33/D34 | CLK0_P |
| +3V3 | | 39 | 40 | F34/E34 | CLK1_N |
| +3V3 | | 41 | 42 | | XRM_SERID |
| +3V3 | | 43 | 44 | | RESERVED |
| +5V | | 45 | 46 | | XRM_VREF |
| +5V | | 47 | 48 | | XRM_VCCIO |
| XRM_VBAT | | 49 | 50 | | XRM_VCCIO |
| +12V | | 51 | 52 | | XRM_VCCIO |
| +12V | | 53 | 54 | | -12V |
| PRESENCE | | 55 | 56 | | XRM_TDI |
| XRM_TCK | | 57 | 58 | | XRM_TRST |
| XRM_TMS | | 59 | 60 | | XRM_TDO |

**Table 10 SX XRM Bus Interface Part 1**

| Signal | FPGA Pin | Samtec Pin | Samtec Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| N_19 | H34 | 61 | 62 | K33 | N_20 |
| P_19 | H33 | 63 | 64 | K32 | P_20 |
| N_21 | P27 | 65 | 66 | K34 | N_22 |
| P_21 | N27 | 67 | 68 | J34 | P_22 |
| N_23 | N30 | 69 | 70 | AF30 | N_24 |
| P_23 | N29 | 71 | 72 | AF29 | P_24 |
| N_25 | AK32 | 73 | 74 | AA28 | P_26 |
| P_25 | AK31 | 75 | 76 | AA29 | N_26 |
| P_27 | W24 | 77 | 78 | AA30 | N_28 |
| N_27 | Y24 | 79 | 80 | AB30 | P_28 |
| N_29 | AE34 | 81 | 82 | AC28 | P_30 |
| P_29 | AE33 | 83 | 84 | AB28 | N_30 |
| N_31 | AC30 | 85 | 86 | AD32 | N_32 |
| P_31 | AC29 | 87 | 88 | AE32 | P_32 |
| CLK2_P | AC32/AD34 | 89 | 90 | AA24 | N_33 |
| CLK3_N | AC33/AC34 | 91 | 92 | AA23 | P_33 |
| N_34 | AF34 | 93 | 94 | AD29 | N_35 |
| P_34 | AF33 | 95 | 96 | AE29 | P_35 |
| CLK4_P | AK24/AL24 | 97 | 98 | AE31 | N_36 |
| CLK5_N | AJ24/AL25 | 99 | 100 | AF31 | P_36 |
| N_37 | AH34 | 101 | 102 | AN22/AM21 | CLK6_P |
| P_37 | AJ34 | 103 | 104 | AN23/AM22 | CLK7_N |
| N_38 | AC27 | 105 | 106 | H32 | S_2 |
| P_38 | AD27 | 107 | 108 | | RESERVED |
| RESERVED | | 109 | 110 | | RESERVED |
| RESERVED | | 111 | 112 | | RESERVED |
| MCLK_N | | 113 | 114 | | RESERVED |
| MCLK_P | | 115 | 116 | | RESERVED |
| RESERVED | | 117 | 118 | | RESERVED |
| RESERVED | | 119 | 120 | | RESERVED |

**Table 11 SX XRM Bus Interface Part 2**

| Signal | FPGA Pin | Samtec Pin | Samtec Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| P_39 | AG30 | 121 | 122 | AH32 | P_40 |
| N_39 | AG31 | 123 | 124 | AH33 | N_40 |
| N_41 | AK34 | 125 | 126 | AM32 | P_42 |
| P_41 | AK33 | 127 | 128 | AM33 | N_42 |
| P_43 | AB22 | 129 | 130 | AL33 | P_44 |
| N_43 | AB23 | 131 | 132 | AL34 | N_44 |
| N_45 | AL31 | 133 | 134 | AH30 | N_46 |
| P_45 | AM31 | 135 | 136 | AJ30 | P_46 |
| P_47 | AG32 | 137 | 138 | AN27 | N_48 |
| N_47 | AG33 | 139 | 140 | AP27 | P_48 |
| P_49 | AP21 | 141 | 142 | AJ29 | N_50 |
| N_49 | AP22 | 143 | 144 | AK29 | P_50 |
| N_51 | AL21 | 145 | 146 | AF26 | P_52 |
| P_51 | AK21 | 147 | 148 | AE26 | N_52 |
| P_53 | AK22 | 149 | 150 | AN30 | N_54 |
| N_53 | AK23 | 151 | 152 | AP30 | P_54 |
| P_55 | AP29 | 153 | 154 | AE27 | N_56 |
| N_55 | AN29 | 155 | 156 | AF28 | P_56 |
| N_57 | AP26 | 157 | 158 | AL30 | N_58 |
| P_57 | AP25 | 159 | 160 | AM30 | P_58 |
| P_59 | AH28 | 161 | 162 | AH27 | N_60 |
| N_59 | AH29 | 163 | 164 | AJ27 | P_60 |
| N_61 | AM27 | 165 | 166 | AL29 | N_62 |
| P_61 | AM26 | 167 | 168 | AL28 | P_62 |
| N_63 | AG26 | 169 | 170 | AN24 | N_64 |
| P_63 | AG25 | 171 | 172 | AP24 | P_64 |
| N_65 | AF24 | 173 | 174 | AK26 | N_66 |
| P_65 | AG23 | 175 | 176 | AL26 | P_66 |
| N_67 | AM25 | 177 | 178 | AM23 | N_68 |
| P_67 | AN25 | 179 | 180 | AL23 | P_68 |

**Table 12 SX XRM Bus Interface Part 3**

Signals marked P_x/N_x and CLKn_P/CLKn+1_N are differential pairs routed for 100R impedance under differential conditions. These can be used single ended if required.
Signals marked S_y are single ended and routed with 50R impedance.

MCLK_P/N is an LVPECL copy of the ADM-XRC-4 MCLK user clock signal. It is terminated on the ADM-XRC-4.

Signals marked with XRM_ are housekeeping signals and are not user programmable.

## 11.4. XRM DCI Option

All three I/O banks that are connected to the XRM interface may optionally use DCI standards where required. The following resistors are fitted to the ADM-XRC-4 to control the impedance.

| Bank | VRP Resistor | VRN Resistor | Value (Ohms) |
|---|---|---|---|
| 9 | R19 | R18 | 49.9 |
| 13 | R20 | R21 | 49.9 |
| 11 | R23 | R22 | 49.9 |

**Table 13 XRM DCI Resistors (LX version)**

| Bank | VRP Resistor | VRN Resistor | Value (Ohms) |
|---|---|---|---|
| 9 | R19 | R18 | 49.9 |
| 11 | R20 | R21 | 49.9 |
| 7 | R23 | R22 | 49.9 |

**Table 14 XRM DCI Resistors (SX version)**

## 11.5. XRM Clocks

There are 8 clock signals available on the XRM interface, organised as 4 pairs. These can be used as inputs or outputs, single-ended or differential (with restrictions).

When inputs are required either of the pins attached to each XRM clock signal can be used. This applies to single or differential signals.

For outputs, either signal pin can be used but only the non-CC pins can be used for differential signalling. Virtex-4 CC pins cannot be used for differential outputs as the circuitry is not present.

| Signal | LX I/O | LX Input CC | FPGA Bank | SX I/O | SX Input CC | FPGA Bank |
|---|---|---|---|---|---|---|
| CLK0 (P) | F33 | D34 | 9 | F33 | D34 | 9 |
| CLK1 (N) | F34 | E34 | 9 | F34 | E34 | 9 |
| CLK2 (P) | R32 | P34 | 13 | AC32 | AD34 | 11 |
| CLK3 (N) | R33 | R34 | 13 | AC33 | AC34 | 11 |
| CLK4 (P) | AG30 | AF29 | 11 | AK24 | AL24 | 7 |
| CLK5 (N) | AG31 | AF30 | 11 | AJ24 | AL25 | 7 |
| CLK6 (P) | AC28 | AA25 | 11 | AN22 | AM21 | 7 |
| CLK7 (N) | AB28 | AA26 | 11 | AN23 | AM22 | 7 |

**Table 15 XRM Clock Pins**

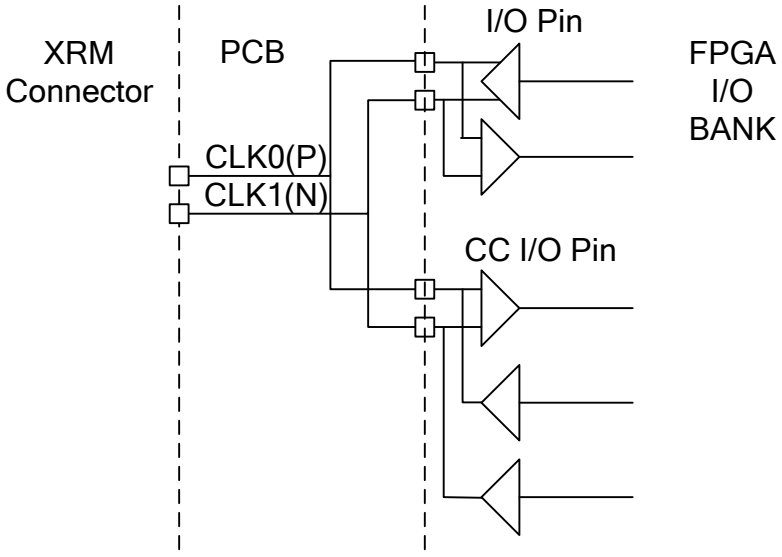



**Figure 4 FPGA XRM Clock Pins**

**Warning**. Care should be taken to ensure that only one of the available two pins on each CLKx signal is active at any one time. It is possible to cause damage to the device because there are no protection resistors present to limit current in the event of contention. See the diagram above for an illustration of CLK0/CLK1 signal configuration.

# 12. Health Monitoring

The ADM-XRC-4 has the ability to monitor temperature and voltage of key parts of the PMC to maintain a check on the operation of the board. The monitoring is implemented by a National Semiconductor LM87 and is supported by the Local Bus control logic Spartan-3 device connected using $I^2C$.

The Control Logic scans the LM87 when instructed by host software and stores all current voltage and temperature measurements in a blockram for reading without the need to communicate directly with the monitor.

The following supplies and temperatures, as shown in Table 16, are monitored.

| Monitor | Purpose |
|---|---|
| 1.2V | User FPGA and Control Logic Core Supply |
| 2.5V | Memory Power and User FPGA Memory I/O |
| 5.0V | Board Input Supply |
| PCI_VIO | Monitors the PCI signalling supply – VIO |
| XRM_VCCIO | Either 2.5V or 3.3V Front Panel I/O Voltage |
| VCC_PN4 | Either 2.5V or 3.3V Pn4 I/O Voltage |
| Temp1 | User FPGA die temperature |
| Temp2 | LM87 on die temperature for board/ambient |

**Table 16 Voltage and Temperature Monitors**

An application is provided in the SDK that permits the reading of the health monitor. The typical output of the monitor is shown below, provided by the SYSMON4 program.

```
Spartan Control Build No.: 01138102

+2V5 Reading    = 2.53 V
Pn4 Reading     = 3.33 V
+5V Reading     = 5.02 V
PCI Vio Reading = 3.31 V
FPIO Reading    = 3.31 V
+1V2 Reading    = 1.20 V

SysMon Int Temp = 35 deg. C
V4 FPGA Temp    = 29 deg. C
```

## 13. JTAG Header – J5

A JTAG header is provided to allow download of the FPGA using the Xilinx tools and serial download cables. This also allows the use of ChipScope PRO ILA to debug an FPGA design. It should be noted that when the SCAN chain is initialised three devices will be detected.

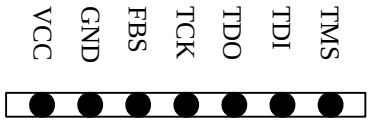



**Figure 5 JTAG Header**

The VCC supply provided on J5 to the JTAG cable is +2.5V and is protected by a poly fuse with a rating of 350mA.

The FBS signal is an input to the control logic and provides control of the cold boot process. By default with no link fitted, the control logic will load a bitstream from flash into the FPGA if one is present. Shorting FBS to the adjacent GND pin will disable this process and can be used to recover situations where rogue bitstreams have been stored in flash.

# 14. XRM IO146 Interface – LX Version

The following tables provide the user with information on the pin-out of the XRM-IO146 when fitted to an ADM-XRC-4/LX version card.

The signal names P_1/N_1 etc are internal to the ADM-XRC-4. The important mapping is between the Mictor pin and the FPGA pin.

| Signal | FPGA Pin | Samtec | Mictor Pin | Mictor Pin | Samtec | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| P_1 | H27 | 3 | 1 | 2 | 6 | N22 | P_4 |
| N_1 | H28 | 1 | 3 | 4 | 8 | N23 | N_4 |
| P_3 | J27 | 7 | 5 | 6 | 4 | C32 | P_2 |
| N_3 | K27 | 5 | 7 | 8 | 2 | D32 | N_2 |
| P_5 | H29 | 11 | 9 | 10 | 12 | J29 | P_6 |
| N_5 | H30 | 9 | 11 | 12 | 10 | J30 | N_6 |
| P_7 | E32 | 15 | 13 | 14 | 16 | P22 | P_8 |
| N_7 | E33 | 13 | 15 | 16 | 14 | R21 | N_8 |
| P_9 | C33 | 17 | 17 | 18 | 18 | K28 | P_10 |
| N_9 | C34 | 19 | 19 | 20 | 20 | K29 | N_10 |
| P_11 | G32 | 23 | 21 | 22 | 24 | L30 | P_12 |
| N_11 | G33 | 21 | 23 | 24 | 22 | L31 | N_12 |
| P_13 | L33 | 27 | 25 | 26 | 26 | M32 | P_14 |
| N_13 | L34 | 25 | 27 | 28 | 28 | M33 | N_14 |
| P_15 | P20 | 31 | 29 | 30 | 30 | L28 | P_16 |
| N_15 | R19 | 29 | 31 | 32 | 32 | L29 | N_16 |
| S_1 | G31 | 37 | 33 | 34 | 38 | D34/F33 | CLK0_P |
| N_34 | T34 | 93 | 35 | 36 | 40 | E34/F34 | CLK1_N |
| +5V | - | - | 37 | 38 | 90 | V34 | N_33 |

| Signal | FPGA Pin | Samtec | Mictor Pin | Mictor Pin | Samtec | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| P_17 | P24 | 35 | 39 | 40 | 36 | M27 | P_18 |
| N_17 | R24 | 33 | 41 | 42 | 34 | M28 | N_18 |
| P_19 | H33 | 63 | 43 | 44 | 64 | K32 | P_20 |
| N_19 | H34 | 61 | 45 | 46 | 62 | K33 | N_20 |
| P_21 | N27 | 67 | 47 | 48 | 68 | J34 | P_22 |
| N_21 | P27 | 65 | 49 | 50 | 66 | K34 | N_22 |
| P_23 | N29 | 71 | 51 | 52 | 72 | W30 | P_24 |
| N_23 | N30 | 69 | 53 | 54 | 70 | V30 | N_24 |
| P_25 | Y32 | 75 | 55 | 56 | 74 | T23 | P_26 |
| N_25 | Y33 | 73 | 57 | 58 | 76 | U23 | N_26 |
| P_27 | R26 | 77 | 59 | 60 | 80 | T24 | P_28 |
| N_27 | T26 | 79 | 61 | 62 | 78 | T25 | N_28 |
| P_29 | P29 | 83 | 63 | 64 | 82 | N32 | P_30 |
| N_29 | R29 | 81 | 65 | 66 | 84 | P32 | N_30 |
| P_31 | P30 | 87 | 67 | 68 | 88 | R31 | P_32 |
| N_31 | P31 | 85 | 69 | 70 | 86 | T31 | N_32 |
| N_38 | U25 | 105 | 71 | 72 | 89 | P34/R32 | CLK2_P |
| P_38 | V25 | 107 | 73 | 74 | 91 | R34/R33 | CLK3_N |
| +5V | - | - | 75 | 76 | 95 | T33 | P_34 |

| Signal | FPGA Pin | Samtec | Mictor Pin | Mictor Pin | Samtec | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| P_37 | U32 | 103 | 77 | 78 | 100 | U30 | P_36 |
| N_37 | U33 | 101 | 79 | 80 | 98 | U31 | N_36 |
| P_39 | V23 | 121 | 81 | 82 | 122 | W32 | P_40 |
| N_39 | V24 | 123 | 83 | 84 | 124 | V32 | N_40 |
| P_41 | W27 | 127 | 85 | 86 | 126 | Y29 | P_42 |
| N_41 | V27 | 125 | 87 | 88 | 128 | W29 | N_42 |
| P_43 | AB32 | 129 | 89 | 90 | 130 | AA33 | P_44 |
| N_43 | AB33 | 131 | 91 | 92 | 132 | AA34 | N_44 |
| P_45 | AB31 | 135 | 93 | 94 | 136 | Y27 | P_46 |
| N_45 | AA31 | 133 | 95 | 96 | 134 | Y28 | N_46 |
| P_47 | T29 | 137 | 97 | 98 | 140 | AJ34 | P_48 |
| N_47 | T30 | 139 | 99 | 100 | 138 | AH34 | N_48 |
| P_49 | AA23 | 141 | 101 | 102 | 144 | AA28 | P_50 |
| N_49 | AA24 | 143 | 103 | 104 | 142 | AA29 | N_50 |
| P_51 | AE33 | 147 | 105 | 106 | 152 | AC29 | P_54 |
| N_51 | AE34 | 145 | 107 | 108 | 150 | AC30 | N_54 |
| P_33 | V33 | 92 | 109 | 110 | 97 | AG30/AF29 | CLK4_P |
| N_35 | U27 | 94 | 111 | 112 | 99 | AG31/AF30 | CLK5_N |
| +5V | - | - | 113 | 114 | - | - | +5V |

| Signal | FPGA Pin | Samtec | Mictor Pin | Mictor Pin | Samtec | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| P_53 | AG32 | 149 | 115 | 116 | 146 | AB30 | P_52 |
| N_53 | AG33 | 151 | 117 | 118 | 148 | AA30 | N_52 |
| P_55 | AD27 | 153 | 119 | 120 | 156 | W24 | P_56 |
| N_55 | AC27 | 155 | 121 | 122 | 154 | Y24 | N_56 |
| P_57 | AE29 | 159 | 123 | 124 | 160 | AE32 | P_58 |
| N_57 | AD29 | 157 | 125 | 126 | 158 | AD32 | N_58 |
| P_59 | AC32 | 161 | 127 | 128 | 164 | AF31 | P_60 |
| N_59 | AC33 | 163 | 129 | 130 | 162 | AE31 | N_60 |
| P_61 | AL33 | 167 | 131 | 132 | 168 | AF33 | P_62 |
| N_61 | AL34 | 165 | 133 | 134 | 166 | AF34 | N_62 |
| P_63 | AH32 | 171 | 135 | 136 | 172 | AB22 | P_64 |
| N_63 | AH33 | 169 | 137 | 138 | 170 | AB23 | N_64 |
| P_65 | AM32 | 175 | 139 | 140 | 176 | AK33 | P_66 |
| N_65 | AM33 | 173 | 141 | 142 | 174 | AK34 | N_66 |
| P_67 | AJ30 | 179 | 143 | 144 | 180 | AM31 | P_68 |
| N_67 | AH30 | 177 | 145 | 146 | 178 | AL31 | N_68 |
| P_35 | U26 | 96 | 147 | 148 | 102 | AA25/AC28 | CLK6_P |
| S_2 | H32 | 106 | 149 | 150 | 104 | AA26/AB28 | CLK7_N |
| +5V | - | - | 151 | 152 | - | - | +5V |

# 15. XRM IO146 Interface – SX Version

The following tables provide the user with information on the pin-out of the XRM-IO146 when fitted to an ADM-XRC-4/SX version card.

The signal names P_1/N_1 etc are internal to the ADM-XRC-4. The important mapping is between the Mictor pin and the FPGA pin.

| Signal | FPGA Pin | Samtec | Mictor Pin | Mictor Pin | Samtec | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| P_1 | H27 | 3 | 1 | 2 | 6 | N22 | P_4 |
| N_1 | H28 | 1 | 3 | 4 | 8 | N23 | N_4 |
| P_3 | J27 | 7 | 5 | 6 | 4 | C32 | P_2 |
| N_3 | K27 | 5 | 7 | 8 | 2 | D32 | N_2 |
| P_5 | H29 | 11 | 9 | 10 | 12 | J29 | P_6 |
| N_5 | H30 | 9 | 11 | 12 | 10 | J30 | N_6 |
| P_7 | E32 | 15 | 13 | 14 | 16 | P22 | P_8 |
| N_7 | E33 | 13 | 15 | 16 | 14 | R21 | N_8 |
| P_9 | C33 | 17 | 17 | 18 | 18 | K28 | P_10 |
| N_9 | C34 | 19 | 19 | 20 | 20 | K29 | N_10 |
| P_11 | G32 | 23 | 21 | 22 | 24 | L30 | P_12 |
| N_11 | G33 | 21 | 23 | 24 | 22 | L31 | N_12 |
| P_13 | L33 | 27 | 25 | 26 | 26 | M32 | P_14 |
| N_13 | L34 | 25 | 27 | 28 | 28 | M33 | N_14 |
| P_15 | P20 | 31 | 29 | 30 | 30 | L28 | P_16 |
| N_15 | R19 | 29 | 31 | 32 | 32 | L29 | N_16 |
| S_1 | G31 | 37 | 33 | 34 | 38 | D34/F33 | CLK0_P |
| N_34 | AF34 | 93 | 35 | 36 | 40 | E34/F34 | CLK1_N |
| +5V | - | - | 37 | 38 | 90 | AA24 | N_33 |

| Signal | FPGA Pin | Samtec | Mictor Pin | Mictor Pin | Samtec | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| P_17 | P24 | 35 | 39 | 40 | 36 | M27 | P_18 |
| N_17 | R24 | 33 | 41 | 42 | 34 | M28 | N_18 |
| P_19 | H33 | 63 | 43 | 44 | 64 | K32 | P_20 |
| N_19 | H34 | 61 | 45 | 46 | 62 | K33 | N_20 |
| P_21 | N27 | 67 | 47 | 48 | 68 | J34 | P_22 |
| N_21 | P27 | 65 | 49 | 50 | 66 | K34 | N_22 |
| P_23 | N29 | 71 | 51 | 52 | 72 | AF29 | P_24 |
| N_23 | N30 | 69 | 53 | 54 | 70 | AF30 | N_24 |
| P_25 | AK31 | 75 | 55 | 56 | 74 | AA28 | P_26 |
| N_25 | AK32 | 73 | 57 | 58 | 76 | AA29 | N_26 |
| P_27 | W24 | 77 | 59 | 60 | 80 | AB30 | P_28 |
| N_27 | Y24 | 79 | 61 | 62 | 78 | AA30 | N_28 |
| P_29 | AE33 | 83 | 63 | 64 | 82 | AC28 | P_30 |
| N_29 | AE34 | 81 | 65 | 66 | 84 | AB28 | N_30 |
| P_31 | AC29 | 87 | 67 | 68 | 88 | AE32 | P_32 |
| N_31 | AC30 | 85 | 69 | 70 | 86 | AD32 | N_32 |
| N_38 | AC27 | 105 | 71 | 72 | 89 | AD34/AC32 | CLK2_P |
| P_38 | AD27 | 107 | 73 | 74 | 91 | AC34/AC33 | CLK3_N |
| +5V | - | - | 75 | 76 | 95 | AF33 | P_34 |

| Signal | FPGA Pin | Samtec | Mictor Pin | Mictor Pin | Samtec | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| P_37 | AJ34 | 103 | 77 | 78 | 100 | AF31 | P_36 |
| N_37 | AH34 | 101 | 79 | 80 | 98 | AE31 | N_36 |
| P_39 | AG30 | 121 | 81 | 82 | 122 | AH32 | P_40 |
| N_39 | AG31 | 123 | 83 | 84 | 124 | AH33 | N_40 |
| P_41 | AK33 | 127 | 85 | 86 | 126 | AM32 | P_42 |
| N_41 | AK34 | 125 | 87 | 88 | 128 | AM33 | N_42 |
| P_43 | AB22 | 129 | 89 | 90 | 130 | AL33 | P_44 |
| N_43 | AB23 | 131 | 91 | 92 | 132 | AL34 | N_44 |
| P_45 | AM31 | 135 | 93 | 94 | 136 | AJ30 | P_46 |
| N_45 | AL31 | 133 | 95 | 96 | 134 | AH30 | N_46 |
| P_47 | AG32 | 137 | 97 | 98 | 140 | AP27 | P_48 |
| N_47 | AG33 | 139 | 99 | 100 | 138 | AN27 | N_48 |
| P_49 | AP21 | 141 | 101 | 102 | 144 | AK29 | P_50 |
| N_49 | AP22 | 143 | 103 | 104 | 142 | AJ29 | N_50 |
| P_51 | AK21 | 147 | 105 | 106 | 152 | AP30 | P_54 |
| N_51 | AL21 | 145 | 107 | 108 | 150 | AN30 | N_54 |
| P_33 | AA23 | 92 | 109 | 110 | 97 | AL24/AK24 | CLK4_P |
| N_35 | AD29 | 94 | 111 | 112 | 99 | AL25/AJ24 | CLK5_N |
| +5V | - | - | 113 | 114 | - | - | +5V |

| Signal | FPGA Pin | Samtec | Mictor Pin | Mictor Pin | Samtec | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| P_53 | AK22 | 149 | 115 | 116 | 146 | AF26 | P_52 |
| N_53 | AK23 | 151 | 117 | 118 | 148 | AE26 | N_52 |
| P_55 | AP29 | 153 | 119 | 120 | 156 | AF28 | P_56 |
| N_55 | AN29 | 155 | 121 | 122 | 154 | AE27 | N_56 |
| P_57 | AP25 | 159 | 123 | 124 | 160 | AM30 | P_58 |
| N_57 | AP26 | 157 | 125 | 126 | 158 | AL30 | N_58 |
| P_59 | AH28 | 161 | 127 | 128 | 164 | AJ27 | P_60 |
| N_59 | AH29 | 163 | 129 | 130 | 162 | AH27 | N_60 |
| P_61 | AM26 | 167 | 131 | 132 | 168 | AL28 | P_62 |
| N_61 | AM27 | 165 | 133 | 134 | 166 | AL29 | N_62 |
| P_63 | AG25 | 171 | 135 | 136 | 172 | AP24 | P_64 |
| N_63 | AG26 | 169 | 137 | 138 | 170 | AN24 | N_64 |
| P_65 | AG23 | 175 | 139 | 140 | 176 | AL26 | P_66 |
| N_65 | AF24 | 173 | 141 | 142 | 174 | AK26 | N_66 |
| P_67 | AN25 | 179 | 143 | 144 | 180 | AL23 | P_68 |
| N_67 | AM25 | 177 | 145 | 146 | 178 | AM23 | N_68 |
| P_35 | AE29 | 96 | 147 | 148 | 102 | AM21/AN22 | CLK6_P |
| S_2 | H32 | 106 | 149 | 150 | 104 | AM22/AN23 | CLK7_N |
| +5V | - | - | 151 | 152 | - | - | +5V |

# 16. XRM IO146A Interface (LX and SX)

The XRM-IO146A is a standard IO module specifically optimised for use with the ADM-XRC-4 series of FPGA processing PMC's.

The XRM-IO146A provides the user with a 152 pin Mictor connector for I/O, compatible with cables from Precision Interconnect. The Mictor connector is referred to in this document as having 4 segments each of 38 pins. These are labelled as M0, M1, M2 and M3 in the following tables and can, with suitable cables, be connected to other XRM cards that implement only 38 pin Mictor connectors.

## 16.1. Specification

| | |
|---|---|
| Number of pairs | 68 |
| Number of clocks | 4 |
| Skew (worst pair) | 100 ps |
| Skew (all pairs) | 100 ps |
| Max data rate | 1Gb/s per pair |
| Battery backup | dual sockets provided |

## 16.2. Terminations

The XRM-IO146A does not use discrete resistors and resistor arrays to terminate LVDS signals but relies on the ability of Virtex-4 devices to provide terminations on-die. If customisation of termination values is required, the XRM-IO146 is a more suitable product.

## 16.3. Resistor Options

There are limited user options on the XRM-IO146A. However, it is possible to modify some characteristics of the board either at the factory or by the user equipped with suitable tools.

### 16.3.1.Reference Voltage

The resistors R11/R13 determine VREF that is fed back to the ADM-XRC-4 via the XRM connector. By default these resistors are each 50R and divide VCCIO by 2.

### 16.3.2.Cable Power

A poly-fuse of 300mA rating is fitted to the board to protect attached cables from damage. If cable power is to be provided, care should be taken in selecting values for R1 to R4 to ensure that the cable is not damaged.

Resistor R1 connects to Mictor pin 37, R2 to pin 75, R3 to pins 113,114 and R4 to pins 151, 152.

## 16.4. Differential Signals with Resistors

A differential pair in each Mictor bank is provided with in line resistors. Each of the signals Mx_P[16]/N[16] has an resistor in series as follows.

| Signal | Resistor – 100R |
|---|---|
| M0_P16 | R7 |
| M0_N16 | R8 |
| M1_P16 | R5 |
| M1_N16 | R6 |
| M2_P16 | R9 |
| M2_N16 | R10 |
| M3_P16 | R14 |
| M3_N16 | R15 |

### 16.5. Clocks and Regions

Virtex-4 devices use clock regions within the device to provide additional clocking resources that are particularly useful for I/O.

The ADM-XRC-4 uses 3 I/O banks to support the XRM interface on the LX (9, 13, 11) and SX (9, 11, 7). Each of the 3 I/O banks is internally adjacent to 2 clock regions giving 6 regions in total. In order to support the 4 Mictor segments (M0,1,2 and 3) shown below the clock and data signals are distributed across the 3 I/O banks and optimised where possible to allow the clock in each segment to capture data using local clocking resources.

| Mictor Bank | Data Signals | LX160 | LX100 | LX80 | SX55 |
|---|---|---|---|---|---|
| M0 | [10:0] | X0Y9 / 9 | X0Y9 / 9 | X0Y7 / 9 | X0Y5 / 9 |
| | [16:11] | X0Y8 / 9 | X0Y8 / 9 | X0Y6 / 9 | X0Y4 / 9 |
| | CLK | X0Y9 / 9 | X0Y9 / 9 | X0Y7 / 9 | X0Y5 / 9 |
| M1 | [5:0] | X0Y8 / 9 | X0Y8 / 9 | X0Y6 / 9 | X0Y4 / 9 |
| | [16:6] | X0Y7 / 13 | X0Y7 / 13 | X0Y5 / 13 | X0Y3 / 11 |
| | CLK | X0Y7 / 13 | X0Y7 / 13 | X0Y5 / 13 | X0Y3 / 11 |
| M2 | [10:0] | X0Y6 / 13 | X0Y6 / 13 | X0Y4 / 13 | X0Y2 / 11 |
| | [12:11] | X0Y2 / 11 | X0Y2 / 11 | X0Y2 / 11 | X0Y0 / 7 |
| | [15:13] | X0Y3 / 11 | X0Y3 / 11 | X0Y3 / 11 | X0Y1 / 7 |
| | CLK | X0Y3 / 11 | X0Y3 / 11 | X0Y3 / 11 | X0Y1 / 7 |
| M3 | 9, [7:3], [1:0] | X0Y3 / 11 | X0Y3 / 11 | X0Y3 / 11 | X0Y1 / 7 |
| | [15:10], 8, 2 | X0Y2 / 11 | X0Y2 / 11 | X0Y2 / 11 | X0Y0 / 7 |
| | 16 | X0Y6 / 13 | X0Y6 / 13 | X0Y4 / 13 | X0Y2 / 11 |
| | CLK | X0Y2 / 11 | X0Y2 / 11 | X0Y3 / 11 | X0Y0 / 7 |

In the case of the LX100 and LX160 it is not possible to capture all of the data signals associated with M2 because of the layout of the regions within the device. Because the clock in M2 is received in region X0Y3, it cannot clock the data signals [10:0] because they are not in an adjacent region. This is not a problem in LX80 and SX55 devices. M2_CLK can otherwise capture data directly on signals connected to regions X0Y2 and X0Y3.

## 16.6. Mictor I/O

The following tables provide the FPGA pin numbers for each of the four segments of the 152 pin Mictor connector. Each segment supports 17 data pairs and one clock.

| LX | SX | Signal | Mictor | | Signal | SX | LX |
|---|---|---|---|---|---|---|---|
| H27 | H27 | M0_P0 | 1 | 2 | M0_P1 | N22 | N22 |
| H28 | H28 | M0_N0 | 3 | 4 | M0_N1 | N23 | N23 |
| J27 | J27 | M0_P2 | 5 | 6 | M0_P3 | C32 | C32 |
| K27 | K27 | M0_N2 | 7 | 8 | M0_N3 | D32 | D32 |
| H29 | H29 | M0_P4 | 9 | 10 | M0_P5 | J29 | J29 |
| H30 | H30 | M0_N4 | 11 | 12 | M0_N5 | J30 | J30 |
| E32 | E32 | M0_P6 | 13 | 14 | M0_P7 | P22 | P22 |
| E33 | E33 | M0_N6 | 15 | 16 | M0_N7 | R21 | R21 |
| C33 | C33 | M0_P8 | 17 | 18 | M0_P9 | K28 | K28 |
| C34 | C34 | M0_N8 | 19 | 20 | M0_N9 | K29 | K29 |
| G32 | G32 | M0_P10 | 21 | 22 | M0_P11 | N29 | N29 |
| G33 | G33 | M0_N10 | 23 | 24 | M0_N11 | N30 | N30 |
| L33 | L33 | M0_P12 | 25 | 26 | M0_P13 | M32 | M32 |
| L34 | L34 | M0_N12 | 27 | 28 | M0_N13 | M33 | M33 |
| P20 | P20 | M0_P14 | 29 | 30 | M0_P15 | L28 | L28 |
| R19 | R19 | M0_N14 | 31 | 32 | M0_N15 | L29 | L29 |
| L30 | L30 | M0_P16 | 33 | 34 | M0_CLK_P | D34,F33 | D34 ,F33 |
| L31 | L31 | M0_N16 | 35 | 36 | M0_CLK_N | E34, F34 | E34, F34 |
| | | +5V | 37 | 38 | Wire_s_1 | G31 | G31 |

| LX | SX | Signal | Mictor | | Signal | SX | LX |
|---|---|---|---|---|---|---|---|
| P24 | P24 | M1_P0 | 39 | 40 | M1_P1 | M27 | M27 |
| R24 | R24 | M1_N0 | 41 | 42 | M1_N1 | M28 | M28 |
| H33 | H33 | M1_P2 | 43 | 44 | M1_P3 | K32 | K32 |
| H34 | H34 | M1_N2 | 45 | 46 | M1_N3 | K33 | K33 |
| N27 | N27 | M1_P4 | 47 | 48 | M1_P5 | J34 | J34 |
| P27 | P27 | M1_N4 | 49 | 50 | M1_N5 | K34 | K34 |
| T33 | AF33 | M1_P6 | 51 | 52 | M1_P7 | AF31 | U30 |
| T34 | AF34 | M1_N6 | 53 | 54 | M1_N7 | AE31 | U31 |
| U26 | AE29 | M1_P8 | 55 | 56 | M1_P9 | AA28 | T23 |
| U27 | AD29 | M1_N8 | 57 | 58 | M1_N9 | AA29 | U23 |
| R26 | W24 | M1_P10 | 59 | 60 | M1_P11 | AB30 | T24 |
| T26 | Y24 | M1_N10 | 61 | 62 | M1_N11 | AA30 | T25 |
| P29 | AE33 | M1_P12 | 63 | 64 | M1_P13 | AC28 | N32 |
| R29 | AE34 | M1_N12 | 65 | 66 | M1_N13 | AB28 | P32 |
| P30 | AC29 | M1_P14 | 67 | 68 | M1_P15 | AE32 | R31 |
| P31 | AC30 | M1_N14 | 69 | 70 | M1_N15 | AD32 | T31 |
| T29 | AG32 | M1_P16 | 71 | 72 | M1_CLK_P | AD34, AC32 | P34, R32 |
| T30 | AG33 | M1_N16 | 73 | 74 | M1_CLK_N | AC34, AC33 | R34, R33 |
| | | +5V | 75 | 76 | Wire_s_2 | H32 | H32 |

| LX | SX | Signal | Mictor | | Signal | SX | LX |
|---|---|---|---|---|---|---|---|
| U32 | AJ34 | M2_P0 | 77 | 78 | M2_P1 | AD27 | V25 |
| U33 | AH34 | M2_N0 | 79 | 80 | M2_N1 | AC27 | U25 |
| V23 | AG30 | M2_P2 | 81 | 82 | M2_P3 | AH32 | W32 |
| V24 | AG31 | M2_N2 | 83 | 84 | M2_N3 | AH33 | V32 |
| W27 | AK33 | M2_P4 | 85 | 86 | M2_P5 | AM32 | Y29 |
| V27 | AK34 | M2_N4 | 87 | 88 | M2_N5 | AM33 | W29 |
| AB32 | AB22 | M2_P6 | 89 | 90 | M2_P7 | AL33 | AA33 |
| AB33 | AB23 | M2_N6 | 91 | 92 | M2_N7 | AL34 | AA34 |
| AB31 | AM31 | M2_P8 | 93 | 94 | M2_P9 | AJ30 | Y27 |
| AA31 | AL31 | M2_N8 | 95 | 96 | M2_N9 | AH30 | Y28 |
| V33 | AA23 | M2_P10 | 97 | 98 | M2_P11 | AP27 | AJ34 |
| V34 | AA24 | M2_N10 | 99 | 100 | M2_N11 | AN27 | AH34 |
| AA23 | AP21 | M2_P12 | 101 | 102 | M2_P13 | AK29 | AA28 |
| AA24 | AP22 | M2_N12 | 103 | 104 | M2_N13 | AJ29 | AA29 |
| AE33 | AK21 | M2_P14 | 105 | 106 | M2_P15 | AP30 | AC29 |
| AE34 | AL21 | M2_N14 | 107 | 108 | M2_N15 | AN30 | AC30 |
| W30 | AF29 | M2_P16 | 109 | 110 | M2_CLK_P | AM21, AN22 | AA25, AC28 |
| V30 | AF30 | M2_N16 | 111 | 112 | M2_CLK_N | AM22, AN23 | AA26, AB28 |
| | | +5V R3 | 113 | 114 | +5V R3 | | |

| LX | SX | Signal | Mictor | | Signal | SX | LX |
|---|---|---|---|---|---|---|---|
| AG32 | AK22 | M3_P0 | 115 | 116 | M3_P1 | AF26 | AB30 |
| AG33 | AK23 | M3_N0 | 117 | 118 | M3_N1 | AE26 | AA30 |
| AD27 | AP29 | M3_P2 | 119 | 120 | M3_P3 | AF28 | W24 |
| AC27 | AN29 | M3_N2 | 121 | 122 | M3_N3 | AE27 | Y24 |
| AE29 | AP25 | M3_P4 | 123 | 124 | M3_P5 | AM30 | AE32 |
| AD29 | AP26 | M3_N4 | 125 | 126 | M3_N5 | AL30 | AD32 |
| AC32 | AH28 | M3_P6 | 127 | 128 | M3_P7 | AJ27 | AF31 |
| AC33 | AH29 | M3_N6 | 129 | 130 | M3_N7 | AH27 | AE31 |
| AL33 | AM26 | M3_P8 | 131 | 132 | M3_P9 | AL28 | AF33 |
| AL34 | AM27 | M3_N8 | 133 | 134 | M3_N9 | AL29 | AF34 |
| AH32 | AG25 | M3_P10 | 135 | 136 | M3_P11 | AP24 | AB22 |
| AH33 | AG26 | M3_N10 | 137 | 138 | M3_N11 | AN24 | AB23 |
| AM32 | AG23 | M3_P12 | 139 | 140 | M3_P13 | AL26 | AK33 |
| AM33 | AF24 | M3_N12 | 141 | 142 | M3_N13 | AK26 | AK34 |
| AJ30 | AN25 | M3_P14 | 143 | 144 | M3_P15 | AL23 | AM31 |
| AH30 | AM25 | M3_N14 | 145 | 146 | M3_N15 | AM23 | AL31 |
| Y32 | AK31 | M3_P16 | 147 | 148 | M3_CLK_P | AL24, AK24 | AF29, AG30 |
| Y33 | AK32 | M3_N16 | 149 | 150 | M3_CLK_N | AL25, AJ24 | AF30, AG31 |
| | | +5V R4 | 151 | 152 | +5V R4 | | |

# 17. Revision History

| Date | Revision | Nature of Change |
|---|---|---|
| 28-09-2005 | 1.0 | Released for printing |
| 29-11-2005 | 1.1 | Minor corrections |
| 24-07-2006 | 1.2 | Fixed Pn4 to FPGA pin numbers on pins 43/44. |
| 06-11-2006 | 1.3 | Included XRM-IO146A chapters |