ADM-XRC-5T2-ADV6

PCI Mezzanine Card

- JPEG2000 Video Compression
- Multi-Gigabit Serial I/O

User Guide

Version 1.0

Alpha Data
4 West Silvermills Lane
Edinburgh EH3 5BD
UK

Phone: +44 (0) 131 558 2600
Fax: +44 (0) 131 558 2700
Email: support@alphadata.co.uk

Alpha Data
2570 North First Street, Suite 440
San Jose, CA 95131
USA

Phone: (408) 467 5076
Fax: (866) 820 9956
Email: support@alpha-data.com

EMI

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

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1. Introduction

The ADM-XRC-5T2-ADV6 is a high performance PCI Mezzanine Card (PMC) designed for supporting development of applications using the Virtex-5 FF1738 Family of FPGA Devices.

- Virtex5 LXT: LX110T, LX155T, LX220T or LX330T
- Virtex 5 SXT: SX240T
- Virtex 5 FXT: FX100T, FX130T, or FX200T

The card uses an FPGA PCI bridge developed by Alpha-Data supporting PCI-X and PCI. A high-speed multiplexed address/data bus connects the bridge to the target (user) FPGA.

The card can also be fitted with a Primary XMC connector to provide high-speed serial links to the user FPGA.

The board is an application specific version of the ADM-XRC-5T2 and features JPEG2000 video compression capabilities and multi-gigabit serial links using 2 FCN x4 Fibre Channel connectors. This board is also an enhanced version of the original ADM-XRC-5T2-ADV board featuring additional JPEG2000 compression hardware.

1.1. Specifications

The ADM-XRC-5T2-ADV6 supports high performance PCI-X / PCI operation without the need to integrate proprietary cores into the FPGA.

- Physically conformant to VITA 42 XMC Standard
- Physically conformant to IEEE P1386-2001 Common Mezzanine Card standard (with XMC connector removed)
- 8-lane PCIe / Serial RapidIO connections to User FPGA (via XMC connector)
- 8 additional MGT links to User FPGA. (via front-panel) A cost-effective solution to applications requiring high-speed data communications such as Infiniband TA, 10G Ethernet, 4x Fibre Channel and others.
- High performance PCI and DMA controllers
- Local bus speeds of up to 80 MHz
- Up to four independent banks of 64Mx32 DDRII SDRAM (1GB total)
- Two banks of 2Mx18 DDRII SSRAM (8MB total)
- User clock programmable between 31.25MHz and 625MHz
- Stable low-jitter 200MHz clock for precision IO delays
- User front panel gigabit serial I/O – 8 lanes in 2 FCN connectors
- 6 JPEG2000 codecs (Analog Devices ADV212) which can be operated individually or in 2 tandem banks to provide compression /decompression of video data
- User rear panel PMC connector with 32 free IO signals
- Programmable I/O voltage rear interfaces
- Supports 3.3V PCI or PCI-X at 64 bits

2. Hardware Installation

This chapter explains how to install the ADM-XRC-5T2-ADV6 onto a PMC motherboard.

2.1. Motherboard requirements

The ADM-XRC-5T2-ADV6 is a 3.3V only PCI device and is not compatible with systems that use 5V PCI signalling levels.

The board must be installed in a PMC motherboard that supplies +5.0V and +3.3V power to the PMC connectors. Ensure that the motherboard satisfies this requirement before powering it up.

2.2. Handling instructions

Observe SSD precautions when handling the cards to prevent damage to components by electrostatic discharge.

Avoid flexing the board.

2.3. Installing the ADM-XRC-5T2-ADV6 onto a PMC motherboard

Note: This operation should not be performed while the PMC motherboard is powered up.

The ADM-XRC-5T2-ADV6 must be secured to the PMC motherboard using M2.5 screws in the four holes provided. The PMC bezel through which the I/O connector protrudes should be flush with the front panel of the PMC motherboard.

2.4. Installing the ADM-XRC-5T2-ADV6 if fitted to an ADC-PMC

The ADM-XRC-5T2-ADV6 can be supplied for use in standard PC systems fitted to an ADC-PMC carrier board. The ADC-PMC can support up to two PMC cards whilst maintaining host PC PCI compatibility. If you are using a ADC-PMC refer to the supplied documentation for information on jumper settings. All that is required for installation is a PCI slot that has enough space to accommodate the full-length card. The ADC-PMC is compatible with 5V and 3V PCI (32 and 64 bit) and PCI-X slots.

It should be noted that the ADC-PMC uses a standard bridge to provide a secondary PCI bus for the ADM-XRC-5T2 and that some older BIOS code does not set up these devices correctly. Please ensure you have the latest version of BIOS appropriate for your machine.

2.5. Installing the ADM-XRC-5T2-ADV6 if fitted to an ADC-EMC

The ADM-XRC-5T2-ADV6 can be supplied for use in standard PC systems fitted to an ADC-EMC carrier board. The ADC-EMC can support up to two PMC cards whilst maintaining host PCI-Express compatibility. If you are using a ADC-EMC refer to the supplied documentation for information on jumper settings. All that is required for installation is a PCIe slot that has enough space to accommodate the full-length card

3. Software Installation

Please refer to the SDK installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

4. Board Description

The ADM-XRC-5T2-ADV6 follows the architecture of the ADM-XRC series and decouples the "target" FPGA from the PCI interface, allowing user applications to be designed with minimum effort and without the complexity of PCI design.

A separate Bridge / Control FPGA interfaces to the PCI bus and provides a simple Local Bus interface to the target FPGA. It also performs all of the board control functions including the configuration of the target FPGA, programmable clock setup and the monitoring of on-board voltage and temperature.

DDR2 SDRAM, SSRAM and serial flash memory connect to the target FPGA and are supported by Xilinx or third party IP.

IO functionality is provided using multi-gigabit I/O connectors and Pn4 signals.

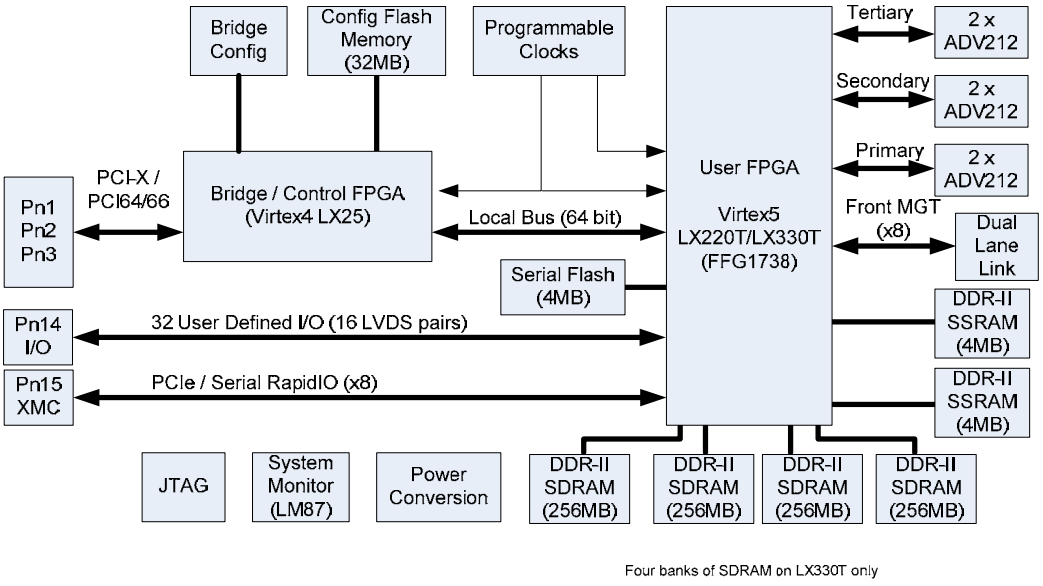

Figure 1 ADM-XRC-5T2-ADV6 Block Diagram

4.1. Local Bus

The ADM-XRC-5T2-ADV6 implements a multi-master local bus between the bridge and the target FPGA using a 32- or 64-bit multiplexed address and data path. The bridge design is asynchronous and allows the local bus to be run faster or slower than the PCI bus clock to suit the requirements of the user design.

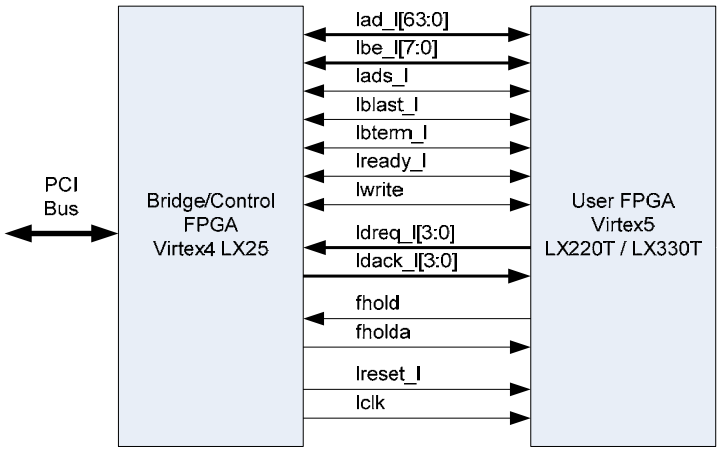

Figure 2 Local Bus Interface

Signal	Type	Purpose
lad[63:0]	bidir	Address and data bus.
lbe_l[7:0]	bidir	Byte qualifiers
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
lwrite	bidir	Indicates a write transfer from master
ldreq_l[3:0]	unidir	DMA request from target to bridge
ldack_l[3:0]	unidir	DMA acknowledge from bridge to target
fhold	unidir	Target bus request
fholda	unidir	Bridge bus acknowledge
lreset_l	unidir	Reset to target
lclk	unidir	Clock to synchronise bridge and target

Table 1 Local Bus Interface Signal List

4.2. Flash Memory

The ADM-XRC-5T2-ADV6 is fitted with two separate Flash memories: one connected to the Bridge / Control FPGA and the other to the User FPGA.

4.2.1. Board Control Flash

A 256Mb Flash memory (Intel / Numonyx PC28F256P30) is used for storing Vital Product Data (VPD), programmable clock parameters and configuration bitstreams for the User FPGA.

Access to this flash device is only possible through control logic registers. The flash is not directly mapped onto the local bus. Programming, erasing and verification of the flash are supported by the ADM-XRC SDK and driver. Utilities are provided to load bitstreams into the flash. These also verify the bitstream is compatible with the target FPGA.

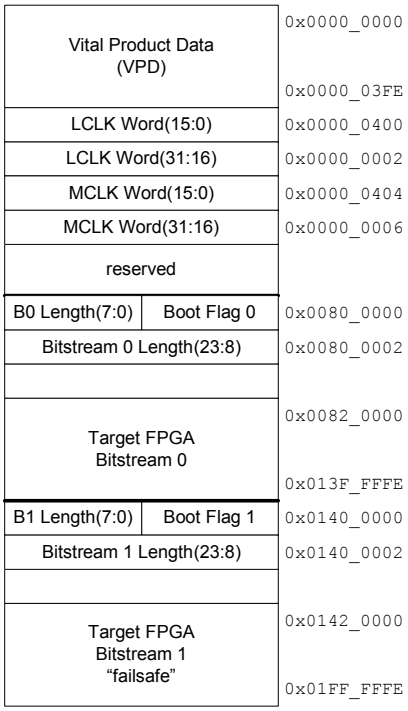

Figure 3 Board Control Flash Organisation

4.2.1.1. Power-Up Sequence

If valid data is stored in the flash memory, the bridge will automatically set the programmable clock generators and configure the User FPGA at power-up.

This sequence can be inhibited by shorting the FBS pin on JTAG connector J2 to GND. See the description of the "FBS" signal in Section 4.4.1 for further information.

Note: If an over-temperature alert is detected from the System Monitor, the target will be reloaded with the alternate (failsafe) bitstream.

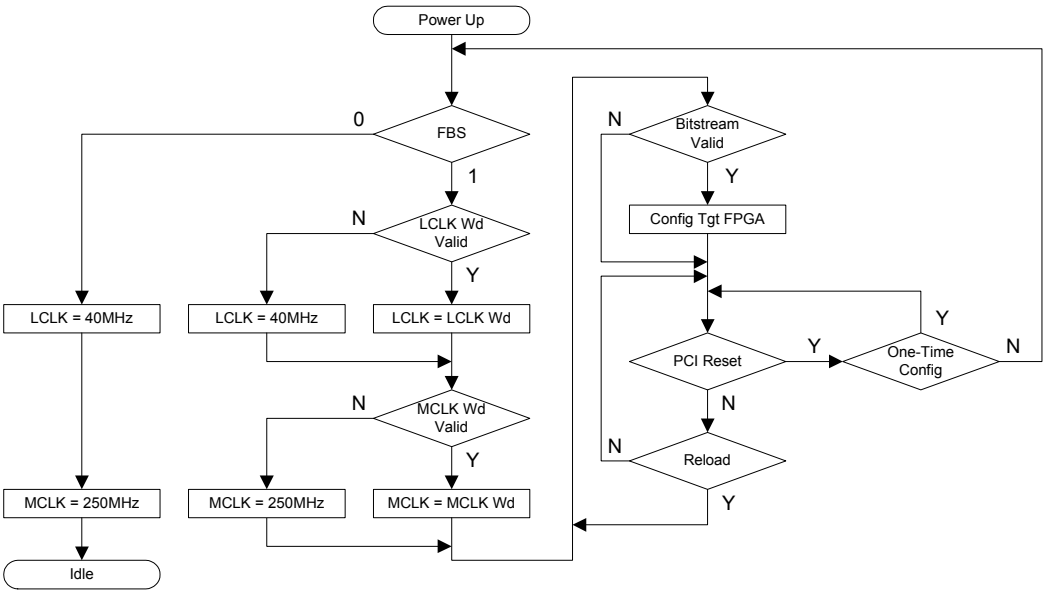

Figure 4 Power-Up Configuration Sequence

4.2.1.2. One-Time Configuration (OTC)

If One-Time Configuration (OTC) is disabled (switch SW1C is OFF), the power-up configuration sequence will repeat each time PCI reset is asserted.

If the OTC feature is enabled (switch SW1C is ON), the bridge will only set the clocks and configure the User FPGA at power-up. Once the sequence has completed, it will not repeat at PCI reset.

Note: OTC only stops the user FPGA being reconfigured at PCI reset. If does not affect the manual reload function in the bridge control registers, or the over-temperature reload circuit

4.2.2. User FPGA Flash

An ST M25P32 flash memory with SPI interface is connected to the User FPGA for the storage of application-specific information.

4.3. Health Monitoring

The ADM-XRC-5T2-ADV6 has the ability to monitor temperature and voltage of key parts of the board to maintain a check on the operation of the board. The monitoring is implemented

by a National Semiconductor LM87 and is supported by the board control logic connected using I^2C.

The Control Logic scans the LM87 when instructed by host software and stores the current voltage and temperature measurements in a blockram. This allows the values to be read without the need to communicate directly with the monitor.

The following supplies and temperatures, as shown in Table 2, are monitored.

Monitor	Purpose
1.0V	User FPGA Core Supply
1.2V	Bridge FPGA Core Supply
1.5V	SRAM and ADV212 Core Supply
1.8V	Memories, User FPGA Memory I/O, Local Bus I/O Config CPLD Core Supply
2.5V	Source voltage for Front, Rear I/O
3.3V	Board Input Supply
5.0V	Board Input Supply
Pn4_VCCIO	Either 2.5V or 3.3V Rear (Pn4) I/O Voltage
Temp1	User FPGA die temperature
Temp2	LM87 on die temperature for board/ambient

Table 2 Voltage and Temperature Monitors

An application is provided in the SDK that permits the reading of the health monitor. The typical output of the monitor is shown below, provided by the SYSMON program.

```
*** SysMon ***

FPGA    Space Base Adr = 00900000
Control Space Base Adr = 00d00000


+1V0 Reading = 1.01 V
+1V2 Reading = 1.21 V
+1V8 Reading = 1.81 V
+2V5 Reading = 2.51 V
+3V3 Reading = 3.32 V
+5V  Reading = 5.04 V
Pn4  Reading = 3.31 V
FPIO Reading = 3.34 V

SysMon Int Temp =   33 deg. C
User FPGA Temp  =   26 deg. C
```

4.3.1. Automatic Temperature Monitoring

At power-up, the control logic sets temperature limits and enables the over-temperature interrupt in the LM87. If the OTC feature is disabled, the limits and interrupt will be re-set after a PCI reset. If OTC is enabled, the limits and interrupt will only be set once at power-up.

The temperature limits are shown in Table 3 below:

	User FPGA		Board (LM87 internal)	
	Min	Max	Min	Max
Commercial	0°C	+85°C	0°C	+70°C
Industrial	-40°C	+100°C	-40°C	+85°C

Table 3 Temperature Limits

If any limit is exceeded, the User FPGA is automatically reconfigured with a low-power "failsafe" bitstream.

The purpose of the failsafe mechanism is to protect the card from damage due to over-heating. It is possible that the reconfiguration will cause the user application and, possibly, the host computer to hang.

There are three ways to determine if the failsafe bitstream has been loaded:

(1) Data bit (30) in the FPCTL control register will be set.
(2) All local bus reads from the user FPGA will return 0xCAFEFABz, where z = Adr(2).
The device USERCODE (readable using JTAG) = 0x4144DEAD.

4.4. JTAG

A JTAG header (J2) is provided to allow download of the FPGA using the Xilinx tools and serial download cables. This also allows the use of ChipScope PRO ILA to debug an FPGA design. It should be noted that four devices will be detected when the SCAN chain is initialised.

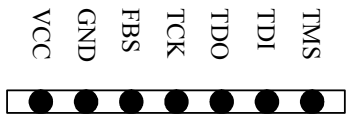

Figure 5 JTAG Header (J2)

The VCC supply provided on J2 to the JTAG cable is +3.3V and is protected by a 350mA poly fuse.

4.4.1. FBS

The FBS signal is an input to the control logic and provides control of the cold boot process. By default with no link fitted, the control logic will load a bitstream from flash into the FPGA if one is present. Shorting FBS to the adjacent GND pin will disable this process and can be used to recover situations where rogue bitstreams have been stored in flash.

4.5. Clocks

The ADM-XRC-5T2-ADV6 is provided with numerous clock sources, as shown in Figure 6 below:

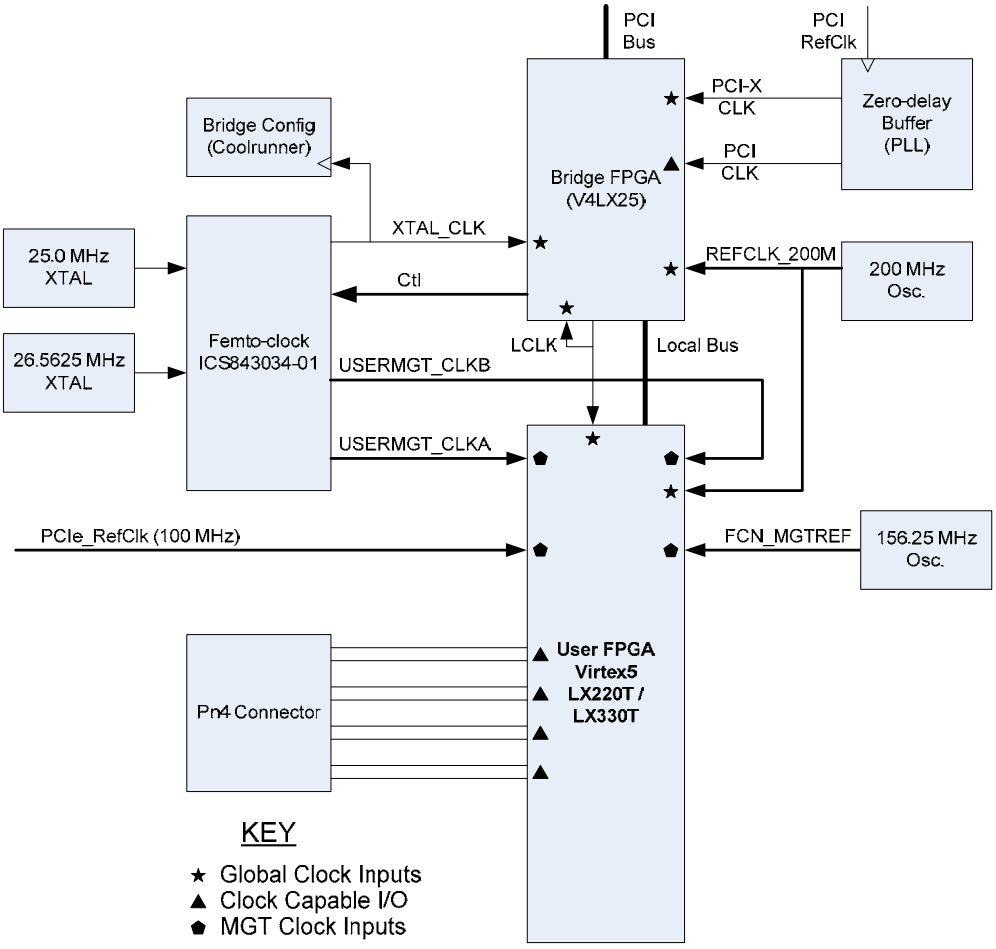

Figure 6 Clock Structure

4.5.1. LCLK

The Local Bus clock, LCLK, is generated from a 200MHz reference by a DCM within the bridge FPGA. The minimum LCLK frequency (determined by the DCM specification) is 32MHz. The maximum is 80MHz.

The LCLK frequency is set by writing DCM multiply & divide values to the LCLOCK register in the bridge. (See SDK for details and example application).

The default LCLK rate is 40MHz and is set on power-up. An alternative default rate can be stored in flash memory:

FlashAdr `0x400` = DCM Multiplier Value – 1
FlashAdr `0x402` = DCM Divider Value – 1

Note: If the user FPGA application includes a DCM driven by LCLK (or one of the other programmable clocks), the clock frequency should be set prior to FPGA configuration.

4.5.2. REFCLK

In order to make use of the IODELAY features of Virtex™-5, a stable low-jitter clock source is required to provide the base timing for tap delay lines in each IOB in the User FPGA. The ADM-XRC-5T2-ADV6 is fitted with a 200MHz LVPECL (LVDS optional) oscillator connected to global clock resource pins. This reference clock can also be used for application logic if required.

4.5.3. PCIe Reference Clock

A 100MHz PCIe reference clock input from the Primary XMC connector (Pn15) is connected to one of the dedicated MGT clock inputs on the user FPGA. (See Table 4 for details of the MGT clock connections.)

Note: This clock is not generated on board. It is only available if the carrier provides it and connector J15 is fitted.

4.5.4. User MGT Clocks

A programmable, low-jitter clock source is provided by an ICS843034-01 “FemtoClocks” frequency synthesiser. The synthesiser has two source crystals – one at 26.5625MHz (for Fibre Channel applications) and another at 25.0MHz (suitable for PCIe, Gigabit Ethernet etc.). The synthesiser also has two clock outputs.

”USERMGT_CLKA” is connected to an MGT clock input on the top-half of the user FPGA. It may be used as an alternative to the PCIe reference for the MGTs connected to the Primary XMC.

”USERMGT_CLKB” is connected to an MGT clock input on the bottom half of the user FPGA. It may be used as the reference for the front user MGTs. (See Table 4 for details of the MGT clock connections.)

Note: Either of these clocks can provide a programmable source for applications that do not use MGTs. This requires the instantiation of a GTP_DUAL component within the FPGA. To simplify the task, a wrapper module is provided in the SDK.

The default rate for both USERMGT_CLKA and USERMGT_CLKB is 250MHz and is set on power-up. An alternative default rate can be stored in flash memory:

FlashAdr `0x404` = ClockWord(15:0)
FlashAdr `0x406` = ClockWord(31:16)

See the ICS843034-01 datasheet for details of the programming clock word.

4.5.5. FCN MGT Clock

A 156.25MHz precision oscillator is fitted on the ADM-XRC-5T2-ADV6 for Gigabit Serial I/O applications. There are also 3 other options for clock inputs to the MGT tiles of the FPGA. The oscillator frequency can be customised to suit applications requiring specific baud rates. Contact the factory for details.

Clock Name	GTP No.	FPGA Pin (P/N)	Reference for:
PCIE_REFCLK	114	AD4 / AD3	Primary XMC (Pn15) MGTs
USERMGT_CLKA	118	AK4 / AK3	Primary XMC (Pn15) MGTs
FCN_MGTREF	124	C4 / C3	Front (CN2) user MGTs
USERMGT_CLKB	112	V4 / V3	Front (CN2) user MGTs

Table 4 MGT Clock Connections

4.5.6. Rear (Pn4) Clocks

Four pairs of signals from Pn4 are connected to clock-capable inputs that can be used for regional clocking of the remaining Pn4 signals. See Table 10 for details.

4.5.7. PCI Clocks

The PCI Interface within the bridge FPGA requires a regional clock input for 66MHz PCI operation or a global clock input for PCI-X. To comply with the single-load requirement in the PCI specification, a zero-delay clock buffer is used to route the PCI clock to the two different clock inputs.

The clock buffer has a PLL with a minimum input frequency of 24MHz, potentially causing problems in applications that use the PCI 33MHz mode with a slow clock. In this case, the buffer can be bypassed to provide full PCI 33MHz compatibility.

4.6. User FPGA

4.6.1. Configuration

The ADM-XRC-5T2-ADV6 performs configuration from the host at high speed using SelectMAP. The FPGA may also be configured from flash or by JTAG via header J2.

Download from the host is the fastest way to configure the User FPGA with 8 bit SelectMAP mode enabled. This permits an ideal configuration speed of up to 80MB/s.

The ADM-XRC-5T2-ADV6 can be configured to boot the User FPGA from flash on power-up if a valid bit-stream is detected in the flash. Booting from flash will also configure the programmable clocks. . See Section 4.2.1.1.

4.6.2. I/O Bank Voltages

Bank	Voltage	Description
0	3.3V	Configuration I/F
1, 4, 5, 6	1.5V	DDRII SRAM
2	3.3V	SelectMAP I/F, Serial Flash
3	3.3V	Clocks
19, 21, 23, 25	1.8V	DDRII DRAM
27, 29, 31, 33	1.8V	DDRII DRAM (LX330T only)
18	2.5V or 3.3V	Pn4 Interface
11, 13, 15, 17, 26, 7, 8, 34	3.3V	ADV212 Interface
12, 20, 24	1.8V	Local Bus

Table 5 User FPGA I/O Bank Voltages

4.6.3. Memory Interfaces

The ADM-XRC-5T2-ADV6 has four independent banks of DDRII SDRAM when fitted with a LX330T, SX240T or FX200T target FPGA. (Two banks with all smaller FPGAs) Each bank consists of two memory devices in parallel to provide a 32 bit datapath. 1Gb Micron MT47H64M16 devices are fitted as standard to provide 256MB per bank. The board will support higher capacity devices when they become available.

The ADM-XRC-5T2-ADV6 has been designed for compatibility with Xilinx memory interface cores.

Details of the signalling standards are given in the table below:

Name	Direction	I/O Standard
DDR_ad[15:0], DDR_ba[2:0], DDR_rasn, DDR_casn, DDR_wen, DDR_csn, DDR_cke, DDR_odt	Output	SSTL18_I_DCI
DDR_ck0, DDR_ckn0	Output	DIFF_SSTL18_II
DDR_dq[15:0]	BiDir	SSTL18_II
DDR_dm[1:0]	Output	SSTL18_II_DCI
DDR_dqs[1:0], DDR_dqsn[1:0]	BiDir	DIFF_SSTL18_II
DDR_ck1, DDR_ckn1	Output	DIFF_SSTL18_II
DDR_dq[31:16]	BiDir	SSTL18_II
DDR_dm[3:2]	Output	SSTL18_II_DCI
DDR_dqs[3:2], DDR_dqsn[3:2]	BiDir	DIFF_SSTL18_II

Table 6 DDR Memory Bank Configuration

4.7. FCN Interface – MGT Links

Eight lanes of user MGT (GTP) links are routed to the front panel connectors. Lanes 0 – 3 are routed through J5, lanes 4 - 7 are routed through J4.

Signal	FPGA Pin	GTP Number	FCN J5 Pin
FCN_TX0_P	AA2	112B	S16
FCN_TX0_N	Y2	"	S15
FCN_RX0_P	Y1	"	S1
FCN_RX0_N	W1	"	S2
FCN_TX1_P	T2	112A	S14
FCN_TX1_N	U2	"	S13
FCN_RX1_P	U1	"	S3
FCN_RX1_N	V1	"	S4
FCN_TX2_P	R2	116B	S12
FCN_TX2_N	P2	"	S11
FCN_RX2_P	P1	"	S5
FCN_RX2_N	N1	"	S6
FCN_TX3_P	K2	116A	S10
FCN_TX3_N	L2	"	S9
FCN_RX3_P	L1	"	S7
FCN_RX3_N	M1	"	S8
Signal	**FPGA Pin**	**GTP Number**	**FCN J4 Pin**
FCN_TX4_P	J2	120B	S16
FCN_TX4_N	H2	"	S15
FCN_RX4_P	H1	"	S1
FCN_RX4_N	G1	"	S2
FCN_TX5_P	D2	120A	S14
FCN_TX5_N	E2	"	S13
FCN_RX5_P	E1	"	S3
FCN_RX5_N	F1	"	S4
FCN_TX6_P	B1	124B	S12
FCN_TX6_N	B2	"	S11
FCN_RX6_P	A2	"	S5
FCN_RX6_N	A3	"	S6
FCN_TX7_P	B6	124A	S10
FCN_TX7_N	B5	"	S9
FCN_RX7_P	A5	"	S7
FCN_RX7_N	A4	"	S8

Table 7 FCN Interface - MGT Links

4.7.1. Copper Mating Cables

Suitable cables are available from Fujitsu "microGiGaCN Cable I/O" range of 8-pair cables in a variety of lengths and styles e.g. FCD-ZZ00001.

Molex provide an alternative source with their 'LaneLink' cables e.g. 74526 -1002

4.7.2. Optical Mating Cables

The optical interface uses external modules which plug in to the standard FCN style connector. These modules (e.g. EMCORE QTR3432) convert the electrical signals to optical format. Inter-module connection uses MJ3MM12RPR-10-0 (available from Fiberconnections Inc.) or similar

Please note that these items are not normally supplied by Alpha Data.

4.7.2.1. Important Notes on using Optical Modules

Optical modules provide a signal ('sense_l') indicating that they are present; however the presence of optical modules cannot be distinguished from a copper connection by relying on this signal alone.

Whilst the optical module supplies are disabled by default and protected by current limiting, the method shown in the example code should always be used to ensure that supplies do not drive into the short circuit presented when a copper cable is fitted.

Caution

This equipment uses Class 1 Laser devices; such devices are not considered to be hazardous when used for their intended purpose. Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous laser light exposure.

4.7.3. Example Gigabit I/O Applications

- Dual Infiniband 4x (4 lanes at 2.5Gb/s over copper or optical fibre)
- Dual 10Gb/s Ethernet CX4 (4 lanes at 3.125Gb/s over copper or optical fibre)
- Dual 10Gb/s FibreChannel (4 lanes at 3.1875Gb/s over copper or optical fibre)
- Dual 4 x OC-48 SONET

4.7.4. Front Panel multi-gigabit I/O Control & Status Signals

Signal	Pin Location	Description
BREFCK_ENAB	AC38	-high to enable the 156.25MHz oscillator on the board (pull-up on board)
STATUS_1	AC40	-Infiniband STATUS led (yellow) connector 1
ATTEN_1	AM42	-Infiniband ATTEN led (green) connector 1
STATUS_2	AC39	-Infiniband STATUS led (yellow) connector 2
ATTEN_2	AM41	-Infiniband ATTEN led (green) connector 2

Table 8 Board Control Signals

Signal	FCN Pin	Connector 1 (J5) FPGA Pin	Connector 2 (J4) FPGA Pin	Description
SENSE	G7	AR5	AM6	low indicates that an opto module has been fitted
FAULT	G6	AT6	AN5	low indicates that no data detected on the opto Rx channel
ODIS	G2	AT7	AN6	low to disable Tx on any module fitted on the channel
PSUEN	G8 (3V3 Pwr)	AP7	AP6	high to enable the opto power supply
OC_L	-	AP5	AL7	low indicates overcurrent on opto supply

Table 9 Optical Module Control Signals

4.8. Pn4 I/O

Up to 16 pairs of differential or 32 single-ended signals are available on Pn4 and are sourced from Bank 18 of the User FPGA. All of the signal traces are routed as 100 Ohm differential pairs and each pair is matched in length. The worst case difference in trace length between any two pairs is 10mm. The pairs are distinguished by the signals names listed below and follow the pattern +/-: 1/3, 2/4, 5/7, 6/8…

Signal	FPGA Pin	Pn4 Pin	Pn4 Pin	FPGA Pin	Signal
PN4_P1	AF11	1	2	AE9	PN4_P2
PN4_N1	AF12	3	4	AE10	PN4_N2
PN4_P3	AF9	5	6	AD8	PN4_P4
PN4_N3	AF10	7	8	AE8	PN4_N4
PN4_P5	AF7	9	10 [CC]	AF5	PN4_P6
PN4_N5	AE7	11	12 [CC]	AF6	PN4_N6
PN4_P7	AC5 [CC]	13	14 [CC]	AB7	PN4_P8
PN4_N7	AC6 [CC]	15	16 [CC]	AB6	PN4_N8
PN4_P9	AG4 [CC]	17	18	AD10	PN4_P10
PN4_N9	AH4 [CC]	19	20	AD11	PN4_N10
PN4_P11	AH6	21	22	AC8	PN4_P12
PN4_N11	AH5	23	24	AC9	PN4_N12
PN4_P13	AB9	25	26	AL5	PN4_P14
PN4_N13	AB8	27	28	AK5	PN4_N14
PN4_P15	AB11	29	30	AJ7	PN4_P16
PN4_N15	AC10	31	32	AK7	PN4_N16

Table 10 Pn4 to FPGA Assignments

In Table 10, pins marked [CC] are clock capable and may be used to access the regional clocking resources in the FPGA.

Banks 18 is fitted with resistors to allow DCI terminations on Pn4 signals.

4.8.1. Pn4 Signalling Voltage

The signalling voltage on the Pn4 connector (and User FPGA Bank 18) is selectable by switch SW2B.

Switch 2B	Pn4 voltage
Open	2.5V
Closed	3.3V

Table 11 Pn4 I/O Voltage Selection

It should be noted that the switch does not directly route power. The switch position is monitored by the board control logic which, in turn, sets a power multiplexer to be either 2.5V or 3.3V.

4.9. XMC Interface

4.9.1. Primary XMC Connector, P15

The MGT (GTP) links connected between the user FPGA and the Primary XMC connector, P15, are compatible with PCI Express and Serial RapidIO. Depending upon the carrier card, they may also be used for user-specific applications.

Signal	FPGA Pin	GTP Number	P15 Pin
PCIE_TX0_P	AB2	114A	A1
PCIE_TX0_N	AC2	"	B1
PCIE_RX0_P	AC1	"	A11
PCIE_RX0_N	AD1	"	B11
PCIE_TX1_P	AG2	114B	D1
PCIE_TX1_N	AF2	"	E1
PCIE_RX1_P	AF1	"	D11
PCIE_RX1_N	AE1	"	E11
PCIE_TX2_P	AH2	118A	A3
PCIE_TX2_N	AJ2	"	B3
PCIE_RX2_P	AJ1	"	A13
PCIE_RX2_N	AK1	"	B13
PCIE_TX3_P	AN2	118B	D3
PCIE_TX3_N	AM2	"	E3
PCIE_RX3_P	AM1	"	D13
PCIE_RX3_N	AL1	"	E13
PCIE_TX4_P	AP2	122A	A5
PCIE_TX4_N	AR2	"	B5
PCIE_RX4_P	AR1	"	A15
PCIE_RX4_N	AT1	"	B15
PCIE_TX5_P	AW2	122B	D5
PCIE_TX5_N	AV2	"	E5
PCIE_RX5_P	AV1	"	D15
PCIE_RX5_N	AU1	"	E15
PCIE_TX6_P	BA1	126A	A7
PCIE_TX6_N	BA2	"	B7
PCIE_RX6_P	BB2	"	A17
PCIE_RX6_N	BB3	"	B17
PCIE_TX7_P	BA6	126B	D7
PCIE_TX7_N	BA5	"	E7
PCIE_RX7_P	BB5	"	D17
PCIE_RX7_N	BB4	"	E17

Table 12 XMC P15 Connections

4.10. ADV212 Interface

The ADV212 is a single-chip JPEG 2000 codec from Analog Devices. It is targeted for video and high bandwidth image compression applications that can benefit from the enhanced quality and features provided by the JPEG 2000 (J2K)—ISO/IEC15444-1 image compression standard. The ADM-XRC-5T2-ADV6 features 6 ADV212 devices which can all operate independently or in 3 banks of 2 for full frame capabilities.

4.10.1. Signal Description

See the ADV212 data sheet and associated literature for a full description of the operation of these pins.

Signals common to each ADV212 bank

addr<1> to <3>	-ADV212 address bus
mclk	-ADV212 system clock
vclk	-ADV212 video data bus clock
hdat<0> to <15>	-ADV212 host data bus
hdat<20> to <31>	-ADV212 host data bus
jpeg_reset_l	-asynchronous processor reset for ADV212's
scomm5	-synchronisation signal for multi-chip operation

Individual signals to each ADV212 codec

ack_l	- ADV212 acknowledge signal
cs_l	- ADV212 chip select signal

dack_l<0> to <1>	- ADV212 DMA acknowledge signals
dreq_l<0> to <1>	- ADV212 DMA request signals
irq_l	- ADV212 interrupt request signal
rd_l	- ADV212 read enable for host interface operation
we_l	- ADV212 write enable for host interface operation
vdat<0> to <15>	- ADV212 video data bus
field	-ADV212 field sync for video mode
hsync	-ADV212 horizontal sync for video mode
vsync	-ADV212 vertical sync for video mode
scom4	- ADV212 LCODE Output in Encode Mode

4.10.2. JPEG Processor Interface Pin Locations

Bank Signals	Bank 1 (A & B)	Bank 2 (C & D)	Bank 3 (E & F)
adv_addr<0>	W35	AJ38	AR25
adv_addr<1>	M41	AJ37	AM21
adv_addr<2>	AA34	AH40	AU26
adv_addr<3>	Y34	AH38	AT24
adv_mclk	T37	AJ42	J23
vclk	Y42	AK8	AP21
jpeg_reset_l	L42	AN41	AT22
scomm5	AF42	AF37	AP22
adv_hdata<0>	AA39	AR40	AT10
adv_hdata<1>	AA41	AT40	AJ22
adv_hdata<2>	AA40	AB34	H19
adv_hdata<3>	AA37	AP40	G19
adv_hdata<4>	AL42	AC34	F19
adv_hdata<5>	AD42	AC35	K20
adv_hdata<6>	Y39	AN40	E20
adv_hdata<7>	Y40	AN39	L21
adv_hdata<8>	AB41	AD35	N22
adv_hdata<9>	Y38	AM39	AK23
adv_hdata<10>	W40	AM38	M23
adv_hdata<11>	AB42	AF39	N23
adv_hdata<12>	W38	AL41	AN23
adv_hdata<13>	V39	AL39	N24
adv_hdata<14>	AD38	AD36	M21
adv_hdata<15>	Y37	AK38	K22
adv_hdata<20>	N41	AC41	AL22
adv_hdata<21>	W37	AC36	AK20
adv_hdata<22>	R39	AB38	AN21
adv_hdata<23>	L40	AF40	AV23
adv_hdata<24>	M42	AE38	AU21
adv_hdata<25>	M39	AR42	AT20
adv_hdata<26>	K38	AP38	AV20
adv_hdata<27>	L39	AE39	AV24
adv_hdata<28>	L41	AD40	AR22
adv_hdata<29>	M38	AT42	AV21
adv_hdata<30>	G39	AU42	AU18
adv_hdata<31>	K39	AD37	AT21

Individual Codec Signals	A	B	C	D	E	F
vdat<0>	J40	AA42	AV5	AM8	AL20	AU9
vdat<1>	K42	AB36	AU6	AM7	F21	AU8
vdat<2>	K40	AB37	AV6	AN8	G21	AT9
vdat<3>	J38	W36	AR8	AL10	E22	AU7
vdat<4>	J42	AA35	AR7	AL6	AL21	AR10
vdat<5>	J41	AA36	AN4	AJ8	G22	AP11
vdat<6>	H39	V40	AN9	AJ11	G23	J20
vdat<7>	H40	W42	AL9	AH11	E23	AL11
vdat<8>	H41	W41	AM9	AH9	F22	AM11
vdat<9>	G41	U41	AG8	AH10	F25	AL12
vdat<10>	F42	U39	AH8	AJ10	G24	AM22
vdat<11>	G42	V41	AP8	AG11	F24	AM23
vdat<12>	AE40	AU12	T41	AV10	L22	AV18
vdat<13>	U38	AU11	AP42	AV8	M22	AW18
vdat<14>	AG38	AV11	P38	AW7	N21	AU17
vdat<15>	AK37	AW12	AG37	AU13	AJ21	AV16
field	F41	AV14	AG12	AW13	AP20	AR13
hsync	E40	AV15	AT5	AR9	AR20	AV13
vsync	F40	AN10	AG9	AP10	AU19	AP12
dack_l<0>	H38	T40	AM37	AK42	H23	AP23
dack_l<1>	F39	U42	AE37	AJ40	G26	AR23
dreq_l<0>	E39	T42	AN38	AK39	H25	AV19
dreq_l<1>	G38	T39	AL37	AT41	F26	AU27
irq_l	R38	N39	AR39	AP41	H21	AR24
scomm4	AH41	AB39	AU41	AF41	J21	F20
cs_l	Y35	N40	AV41	AG42	J22	AT25
rd_l	R37	P40	AU39	AD41	H24	AK22
we_l	P37	P41	AV40	AE42	K23	AV25
ack_l	N38	R40	AT39	AG41	H20	AU24

5. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

6. Revision History

Date	Revision	Nature of Change
14-Dec-2009	0.1	Initial version – based on 5T2-ADV manual
17-Dec-2009	1.0	Bridge functionality updates from current 5T2 - Extended flash boot description - Not on auto temp monitoring - Different LCLK/MCLK default values supported - PCIe ref clock provision – Pn15 - Configuration speed update – 80MB/s