ADM-XRC-5TZ

PCI Mezzanine Card

User Guide

Version 2.0

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1. Introduction

The ADM-XRC-5TZ is a high performance PCI Mezzanine Card (PMC) designed for applications using the Virtex-5 FPGAs from Xilinx. This card supports all Virtex-5 LXT, SXT and FXT devices with the FFG1738 package.

The card uses an FPGA PCI bridge developed by Alpha-Data supporting PCI-X and PCI. This allows high performance PCI-X / PCI operation without the need to integrate proprietary cores into the FPGA.

A high-speed multiplexed address/data bus connects the bridge to the target (user) FPGA.

The card can also be fitted with a Primary XMC connector to provide high-speed serial link connections to the user FPGA.

1.1. Specifications

- Physically conformant to VITA 42 XMC Standard
- Physically conformant to IEEE P1386-2001 Common Mezzanine Card standard (with XMC connector removed)
- 8-lane PCIe / Serial RapidIO connections to User FPGA (via XMC connector)
- 8 additional MGT links to User FPGA. (via front-panel adaptor)
- High performance PCI and DMA controllers
- Local bus speeds of up to 80 MHz
- Six independent banks of 2Mx36 ZBT SRAM (48MB total)
- User clock programmable between 31.25MHz and 625MHz
- Stable low-jitter 200MHz clock for precision IO delays
- User front panel adapter with up to 146 free IO signals
- User rear panel PMC connector with 6 free IO signals
- Programmable I/O voltage on front interface (1.8V / 2.5V / 3.3V)
- Supports 3.3V PCI or PCI-X at 64 bits

2. Hardware Installation

This chapter explains how to install the ADM-XRC-5TZ onto a PMC motherboard or carrier.

2.1. Handling instructions

Observe SSD precautions when handling the cards to prevent damage to components by electrostatic discharge.

Avoid flexing the board.

2.2. Motherboard / Carrier requirements

The ADM-XRC-5TZ is a 3.3V only PCI device and is not compatible with systems that use 5V signalling.

The ADM-XRC-5TZ must be installed in a PMC motherboard or carrier that supplies +5.0V and +3.3V power to the PMC connectors. Ensure that this requirement is satisfied before powering it up. +12V and -12V may also be required for certain XRM modules.

The current requirements on each power rail are highly dependent on the user FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact requirements for each power rail.

2.3. PCI Mode selection

Although the ADM-XRC-5TZ automatically detects whether the board is connected to a PCI or PCI-X bus, the default (initial) type is determined by Switch SW1D.

If SW1D is OFF, the bridge FPGA will be configured for PCI-X mode after power-up and altered at PCI reset if a PCI bus is detected.

If SW1D is ON, the bridge FPGA will be configured for PCI mode after power-up and altered at PCI reset if a PCI-X bus is detected.

In most systems it is not essential to alter the position of this switch. However, systems with a PCIe interface in the User FPGA should load the user bitstream in to flash memory, set SW1D to match the bus type and enable the One-Time Configuration (OTC) feature (by setting SW1A to ON). See Section 4.2.1.2 for more details on OTC.

2.4. Installing the ADM-XRC-5TZ onto a PMC motherboard

Note: This operation should not be performed while the PMC motherboard is powered up.

The ADM-XRC-5TZ must be secured to the PMC motherboard using M2.5 screws in the four holes provided. The PMC bezel through which the I/O connector protrudes should be flush with the front panel of the PMC motherboard.

2.5. Installing the ADM-XRC-5TZ if fitted to an ADC-PMC

The ADM-XRC-5TZ can be supplied for use in standard PC systems fitted to an ADC-PMC carrier board. The ADC-PMC can support up to two PMC cards whilst maintaining host PC PCI compatibility. If you are using a ADC-PMC, refer to the supplied documentation for information on jumper settings. All that is required for installation is a PCI slot that has enough space to accommodate the full-length card. The ADC-PMC is compatible with 5V and 3V PCI (32 and 64 bit) and PCI-X slots.

It should be noted that the ADC-PMC uses a standard bridge to provide a secondary PCI bus for the ADM-XRC-5TZ and that some older BIOS code does not set up these devices correctly. Please ensure you have the latest version of BIOS appropriate for your machine.

2.6. Cooling Requirements

The power consumption of the ADM-XRC-5TZ is highly dependent on the user FPGA application. With large FPGA applications, it is possible that the board may dissipate more than 15W. Although the board is designed to handle this, the user must ensure that it is adequately cooled.

To prevent damage through over-heating, an on-board system monitor will automatically reconfigure the User FPGA with a low-power bitstream if the FPGA reaches 85°C or if the board reaches 70°C. (100°C and 85°C respectively for Industrial grade devices).

The FPGA temperature may be measured using a software application or with Xilinx Chipscope and a JTAG cable.

See Section 4.3 for further details of the on-board system monitor.

3. Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

4. Board Description

The ADM-XRC-5TZ follows the architecture of the ADM-XRC series and decouples the "target" FPGA from the PCI interface, allowing user applications to be designed with minimum effort and without the complexity of PCI design.

A separate Bridge / Control FPGA interfaces to the PCI bus and provides a simpler Local Bus interface to the target FPGA. It also performs all of the board control functions including the configuration of the target FPGA, programmable clock setup and the monitoring of on-board voltage and temperature.

ZBT SRAM and serial flash memory connect to the target FPGA and are supported by Alpha Data or Xilinx IP.

IO functionality is provided using XRM modules. MGT links are connected through a SAMTEC QSE-DP connector, CN2. Remaining signals are connected through a 180 pin SAMTEC QSH connector, CN1.

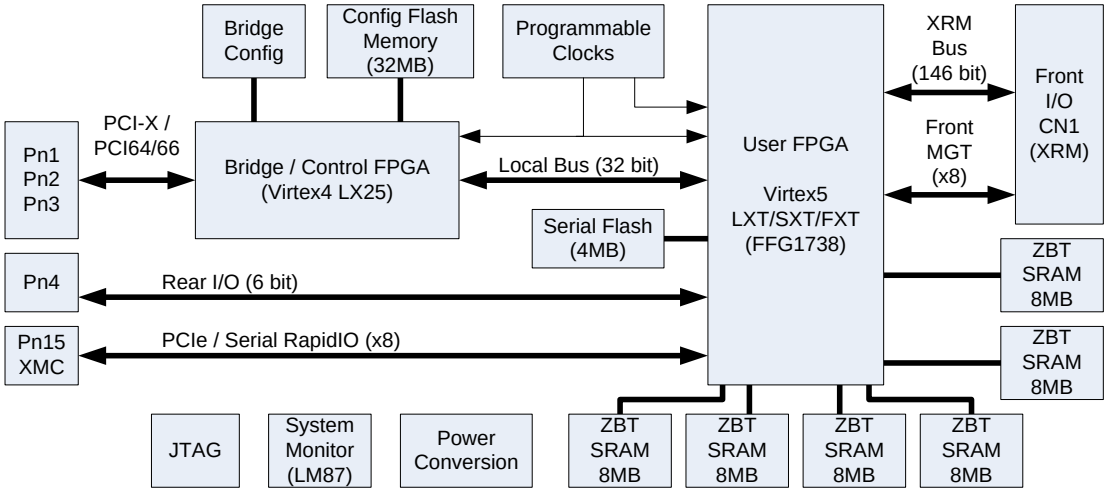

Figure 1 ADM-XRC-5TZ Block Diagram

4.1. Local Bus

The ADM-XRC-5TZ implements a multi-master local bus between the bridge and the target FPGA using a 32-bit multiplexed address / data path. The bridge design is asynchronous and allows the local bus to be run faster or slower than the PCI bus clock to suit the requirements of the user design.

The local bus runs at 40MHz by default but this can be altered to different frequencies between 32MHz and 80MHz.

Full details of the local bus operation, including timing constraints, DMA and Interrupts are given in the Software Development Kit (SDK).

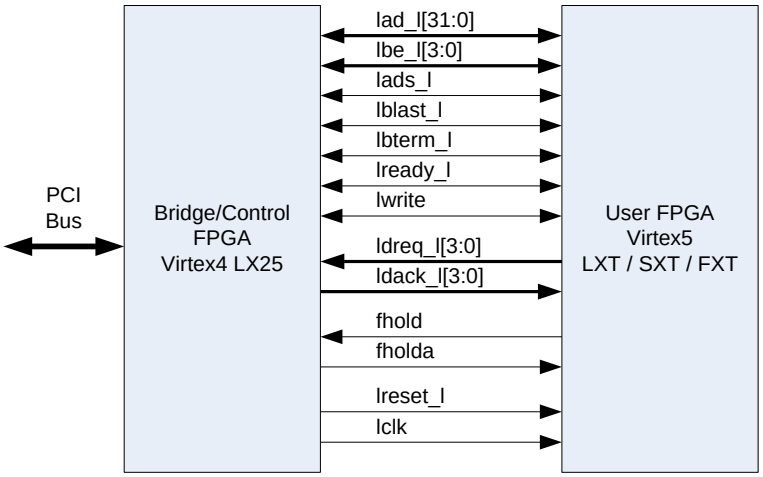

Figure 2 Local Bus Interface

Signal	Type	Purpose
lad[31:0]	bidir	Address and data bus.
lbe_l[3:0]	bidir	Byte qualifiers
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
lwrite	bidir	Indicates a write transfer from master
ldreq_l[3:0]	unidir	DMA request from target to bridge
ldack_l[3:0]	unidir	DMA acknowledge from bridge to target
fhold	unidir	Target bus request
fholda	unidir	Bridge bus acknowledge
lreset_l	unidir	Reset to target
lclk	unidir	Clock to synchronise bridge and target

Table 1 Local Bus Interface Signal List

4.2. Flash Memory

The ADM-XRC-5TZ is fitted with two separate Flash memories: one connected to the Bridge / Control FPGA and the other to the User FPGA.

4.2.1. Board Control Flash

A 256Mb Flash memory (Intel / Numonyx PC28F256P30) is used for storing Vital Product Data (VPD), programmable clock parameters and configuration bitstreams for the User FPGA.

Access to this flash device is only possible through control logic registers. The flash is not directly mapped onto the local bus. Programming, erasing and verification of the flash are supported by the ADM-XRC SDK and driver. Utilities are provided to load bitstreams into the flash. These also verify the bitstream is compatible with the target FPGA.

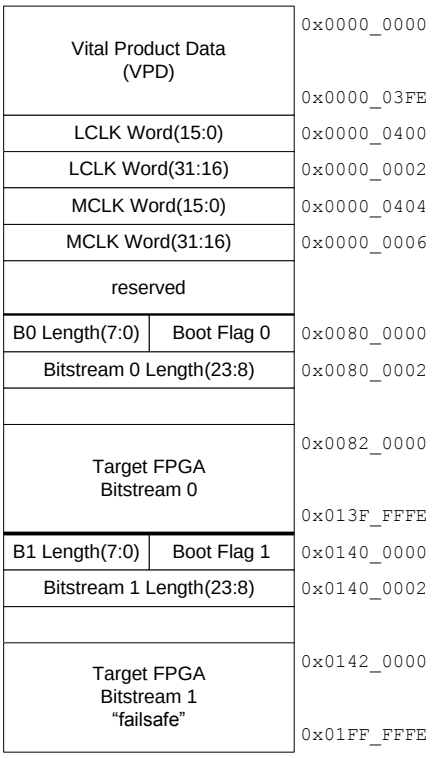

Figure 3 Board Control Flash Organisation

4.2.1.1. Power-Up Sequence

If valid data is stored in the flash memory, the bridge will automatically set the programmable clock generators and configure the User FPGA at power-up.

This sequence can be inhibited by shorting the FBS pin on JTAG connector J3 to GND. See the description of the "FBS" signal in Section 4.4 for further information.

Note: If an over-temperature alert is detected from the System Monitor, the target will be reloaded with the alternate (failsafe) bitstream.

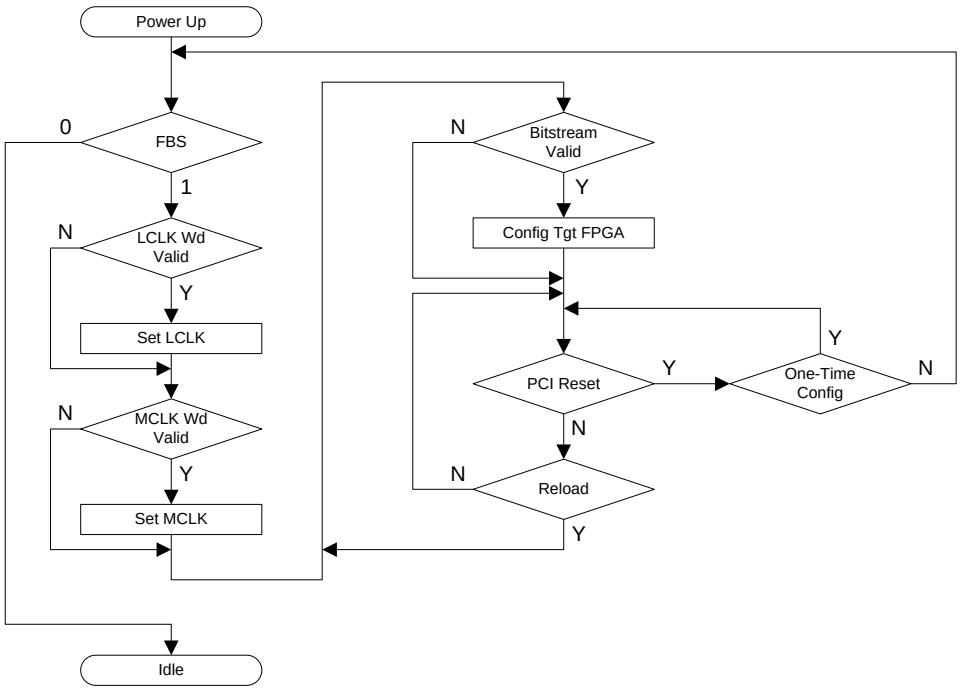

Figure 4 Power-Up Configuration Sequence

4.2.1.2. One-Time Configuration (OTC)

If One-Time Configuration (OTC) is disabled (switch SW1A is OFF), the power-up configuration sequence will repeat each time PCI reset is asserted.

If the OTC feature is enabled (switch SW1A is ON), the bridge will only set the clocks and configure the User FPGA at power-up. Once the sequence has completed, it will not repeat at PCI reset.

Note: OTC only stops the user FPGA being reconfigured at PCI reset. If does not affect the manual reload function in the bridge control registers, or the over-temperature reload circuit.

4.2.2. User FPGA Flash

An ST M25P32 flash memory with SPI interface is connected to the User FPGA for the storage of application-specific information.

4.3. Health Monitoring

The ADM-XRC-5TZ has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented by a National Semiconductor LM87 and is supported by the Bridge FPGA control logic using I^2C.

The Control Logic scans the LM87 when instructed by host software and stores the current voltage and temperature measurements in a blockram. This allows the values to be read without the need to communicate directly with the monitor.

The following supplies and temperatures, as shown in Table 2, are monitored.

Monitor	Purpose
1.0V	User FPGA Core Supply
1.2V	Bridge FPGA Core Supply
1.8V	Memories, User FPGA Memory I/O, Local Bus I/O Config CPLD Core Supply
2.5V	Source voltage for Front, Rear I/O
3.0V	PCI VIO voltage (for Bridge FPGA)
3.3V	Board Input Supply
5.0V	Board Input Supply
XRM_VCCIO	Either 2.5V or 3.3V Front Panel I/O Voltage
Temp1	User FPGA die temperature
Temp2	LM87 on die temperature for board/ambient

Table 2 Voltage and Temperature Monitors

An application is provided in the SDK that permits the reading of the health monitor. The typical output of the monitor is shown below, provided by the SYSMON program.

```
*** SysMon ***

FPGA    Space Base Adr = 00900000
Control Space Base Adr = 00d00000


+1V0 Reading = 1.01 V
+1V2 Reading = 1.21 V
+1V8 Reading = 1.81 V
+2V5 Reading = 2.51 V
+3V0 Reading = 3.01 V
+5V  Reading = 5.04 V
FPIO Reading = 3.34 V

SysMon Int Temp =   33 deg. C
User FPGA Temp  =   26 deg. C
```

4.3.1. Automatic Temperature Monitoring

At power-up, the control logic sets temperature limits and enables the over-temperature interrupt in the LM87. If the OTC feature is disabled, the limits and interrupt will be re-set after a PCI reset. If OTC is enabled, the limits and interrupt will only be set once at power-up.

The temperature limits are shown in Table 3 below:

	User FPGA		Board (LM87 internal)	
	Min	Max	Min	Max
Commercial	0°C	+85°C	0°C	+70°C
Industrial	-40°C	+100°C	-40°C	+85°C

Table 3 Temperature Limits

If any limit is exceeded, the User FPGA is automatically reconfigured with a low-power "failsafe" bitstream.

The purpose of the failsafe mechanism is to protect the card from damage due to over-heating. It is possible that the reconfiguration will cause the user application and, possibly, the host computer to hang.

There are three ways to determine if the failsafe bitstream has been loaded:

(1) Data bit (30) in the FPCTL control register will be set.
(2) All local bus reads from the user FPGA will return 0xCAFEFABz, where z = Adr(2).
(3) The device USERCODE (readable using JTAG) = 0x4144DEAD.

4.4. JTAG

A JTAG header (J3) is provided to allow download of the FPGA using the Xilinx tools and serial download cables. This also allows the use of ChipScope PRO ILA to debug an FPGA design.

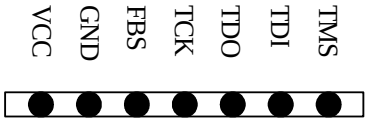

Figure 5 JTAG Header J3

The VCC supply provided on J3 to the JTAG cable is +3.3V and is protected by a poly fuse with a rating of 350mA.

4.4.1. Scan Chain Options

The devices in the scan chain can be altered for board test purposes using switch SW1C. The normal position for SW1C is open (off). In this position, four devices will be detected when the scan chain is initialised.

If SW1C is closed (on), the ZBT memories will be included in the scan chain.

4.4.2. FBS

The FBS signal is an input to the control logic and provides control of the cold boot process. By default, with no link fitted, the control logic will load a bitstream from flash into the FPGA if one is present. Shorting FBS to the adjacent GND pin will disable this process and can be used to recover situations where rogue bitstreams have been stored in flash.

4.5. Clocks

The ADM-XRC-5TZ is provided with numerous clock sources, as shown in Figure 6 below:

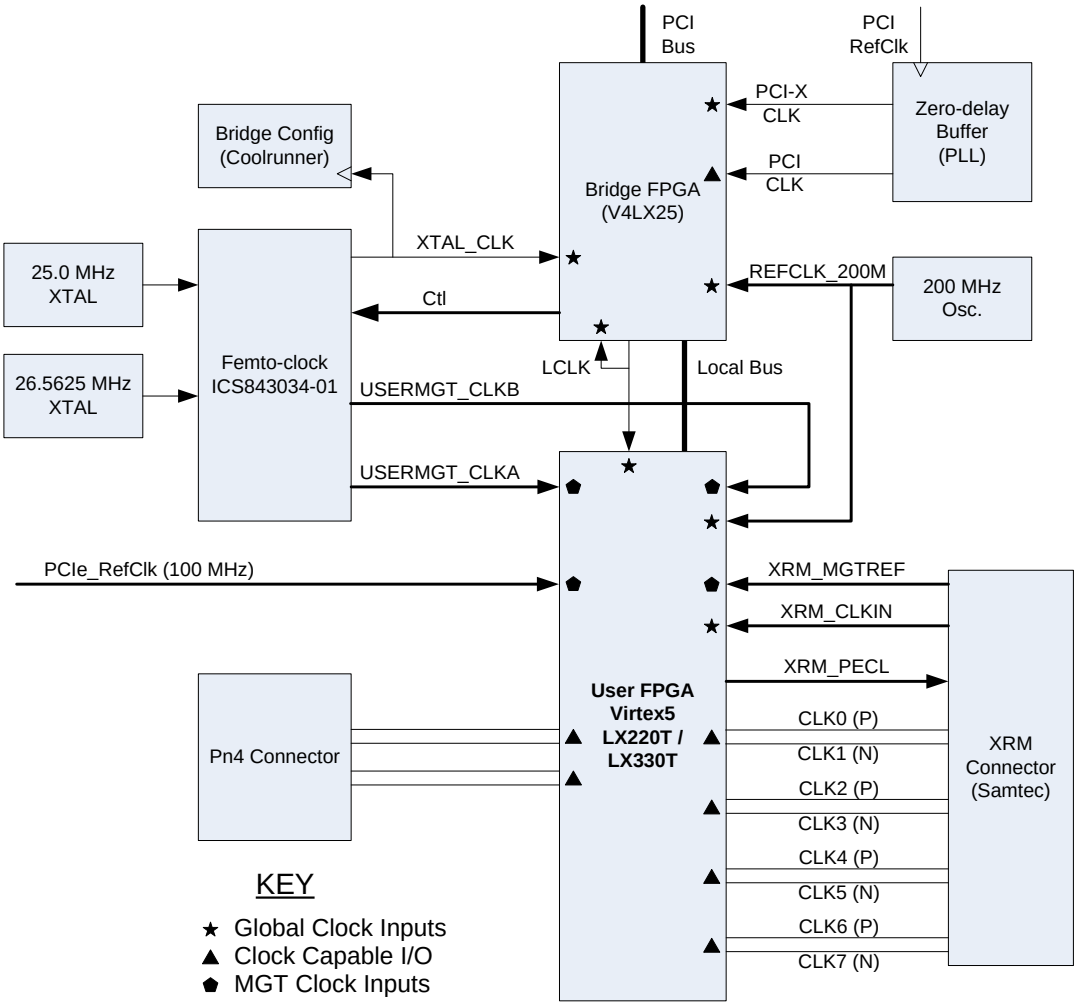

Figure 6 Clock Structure

4.5.1. LCLK

The Local Bus clock, LCLK, is generated from a 200MHz reference by a DCM within the bridge FPGA. The minimum LCLK frequency (determined by the DCM specification) is 32MHz. The maximum is 80MHz.

The LCLK frequency is set by writing DCM multiply & divide values to the LCLOCK register in the bridge. (See SDK for details and example application).

The default LCLK rate is 40MHz and is set on power-up. An alternative default rate can be stored in flash memory:

FlashAdr `0x400` = DCM Multiplier Value – 1
FlashAdr `0x402` = DCM Divider Value – 1

Note: If the user FPGA application includes a DCM driven by LCLK (or one of the other programmable clocks), the clock frequency should be set prior to FPGA configuration.

4.5.2. REFCLK

In order to make use of the IODELAY features of Virtex™-5, a stable low-jitter clock source is required to provide the base timing for tap delay lines in each IOB in the User FPGA. The ADM-XRC-5TZ is fitted with a 200MHz LVPECL (LVDS optional) oscillator connected to global clock resource pins. This reference clock can also be used for application logic if required.

4.5.3. PCIe Reference Clock

A 100MHz PCIe reference clock input from the Primary XMC connector (Pn15) is connected to one of the dedicated MGT clock inputs on the user FPGA. (See Table 4 for details of the MGT clock connections.)

Note: This clock is not generated on board. It is only available if the carrier provides it and connector Pn15 is fitted.

4.5.4. User MGT Clocks

A programmable, low-jitter clock source is provided by an ICS843034-01 “FemtoClocks” frequency synthesiser. The synthesiser has two source crystals – one at 26.5625MHz (for Fibre Channel applications) and another at 25.0MHz (suitable for PCIe, Gigabit Ethernet etc.). The synthesiser also has two clock outputs.

”USERMGT_CLKA” is connected to an MGT clock input on the top-half of the user FPGA. It may be used as an alternative to the PCIe reference for the MGTs connected to the Primary XMC.

”USERMGT_CLKB” is connected to an MGT clock input on the bottom half of the user FPGA. It may be used as the reference for the front user MGTs. (See Table 4 for details of the MGT clock connections.)

Note: Either of these clocks can provide a programmable source for applications that do not use MGTs. This requires the instantiation of a GTP_DUAL component within the FPGA. To simplify the task, a wrapper module is provided in the SDK.

The default rate for both USERMGT_CLKA and USERMGT_CLKB is 250MHz and is set on power-up. An alternative default rate can be stored in flash memory:

FlashAdr `0x404` = ClockWord(15:0)
FlashAdr `0x406` = ClockWord(31:16)

See the ICS843034-01 datasheet for details of the programming clock word.

4.5.5. XRM MGT Clock

An XRM module can provide an MGT (GTP) reference clock input for user-specific applications.

Clock Name	GTP No.	FPGA Pin (P/N)	Reference for:
PCIE_REFCLK	114	AD4 / AD3	Primary XMC (Pn15) MGTs
USERMGT_CLKA	118	AK4 / AK3	Primary XMC (Pn15) MGTs
XRM_MGTREF	124	C4 / C3	Front (CN2) user MGTs
USERMGT_CLKB	112	V4 / V3	Front (CN2) user MGTs

Table 4 MGT Clock Connections

4.5.6. XRM Global Clock Input

The XRM interface provides a differential input to the User FPGA global clocking resources. The default on-board terminations are suitable for an LVDS clock.

4.5.7. XRM Regional Clocks

The XRM interface provides 8 clock lines that can be either be used single-ended or as 4 LVDS differential pairs. These clocks are routed to Clock-Capable inputs on the User FPGA, providing access to its regional clock capabilities.

Each clock pair can be coupled with 16 pairs of XRM bus signals, as shown in Table 5 below:

XRM Clocks	FPGA Bank	XRM bus pairs
0 & 1 (Pair 0)	15	1 – 16
2 & 3 (Pair 1)	11	17 – 32
4 & 5 (Pair 2)	13	33 – 48
6 & 7 (Pair 3)	17	49 – 64

Table 5 XRM Bus Regional Clocks

4.5.8. Rear (Pn4) Clocks

Two pairs of signals from Pn4 are connected to clock-capable inputs that can be used for regional clocking of the remaining Pn4 signals. See Table 12 for details.

4.5.9. PCI Clocks

The PCI Interface within the bridge FPGA requires a regional clock input for 66MHz PCI operation or a global clock input for PCI-X. To comply with the single-load requirement in the PCI specification, a zero-delay clock buffer is used to route the PCI clock to the two different clock inputs.

The clock buffer has a PLL with a minimum input frequency of 24MHz, potentially causing problems in applications that use the PCI 33MHz mode with a slow clock. In this case, the buffer can be bypassed to provide full PCI 33MHz compatibility.

4.6. User FPGA

4.6.1. Configuration

The ADM-XRC-5TZ performs configuration from the host at high speed using SelectMAP. The FPGA may also be configured from flash or by JTAG via header J3.

Download from the host is the fastest way to configure the User FPGA with 8 bit SelectMAP mode enabled. This permits an ideal configuration speed of up to 80MB/s.

The ADM-XRC-5TZ can be configured to boot the User FPGA from flash on power-up if a valid bit-stream is detected in the flash. Booting from flash will also configure the programmable clocks. See Section 4.2.1.1.

4.6.2. I/O Bank Voltages

Bank	Voltage	Description
0	3.3V	Configuration I/F
1, 5, 6, 18, 19, 21, 23, 24, 25, 26	2.5V	ZBT SRAM
2	3.3V	SelectMAP I/F, Pn4, Serial Flash
3, 4	2.5V	Clocks, ZBT SRAM
11, 13, 15, 17	1.8V, 2.5V or 3.3V	XRM Interface
12, 20	2.5V	Local Bus

Table 6 User FPGA I/O Bank Voltages

4.6.3. Memory Interfaces

The ADM-XRC-5TZ has six independent banks of ZBT SRAM. Each bank has a 36 bit datapath. Data bits (35:32) are parity bits, where bit 32 is associated with bits (7:0) etc.

The board will support higher capacity devices when they become available.

4.6.3.1. Memory Clocking

Each memory bank has its own clock output from the target FPGA. To allow these clocks to be de-skewed, they are fed back into GCLK inputs on the FPGA.

An example of this clock de-skewing method is shown in the “memory” application in the Alpha Data SDK.

4.7. XRM Bus and Front Panel I/O

A major benefit of the ADM-XRC series of boards that use the XRM Bus interface is the versatility of I/O options that result. The ADM-XRC-5TZ maintains this interface and thus compatibility with a wide range of I/O modules to suit many diverse needs.

Standard signals and power on the XRM interface use the 180 pin Samtec QSH series connector, CN1. MGT links use the 28 pin Samtec QSE-DP connector, CN2.

4.7.1. XRM Signalling Voltage

The signalling voltage on the XRM connector (and User FPGA Banks 11, 13, 15 & 17) is selectable by jumper J2

J2	XRM I/O voltage
Link p1 & p2	3.3V
Link p3 & p4	2.5V
Link p5 & p4	1.8V

Table 7 XRM I/O Voltage Selection

4.7.2. XRM Interface – Standard Signals and Power

The XRM interface is implemented on CN1, a 180 pin Samtec connector type QSH, with the pin-out as detailed in tables Table 8 to Table 10.

In turn, the signals that connect to CN1 are provided in the main from four banks of the User FPGA, Banks 11, 13, 15 & 17. These banks share a common VCCO that can be 1.8V, 2.5V or 3.3V powered, selectable with a jumper link on J3.

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
N_1	H39	1	2	G39	N_2
P_1	H38	3	4	G38	P_2
N_3	F40	5	6	E39	P_4
P_3	F39	7	8	E40	N_4
N_5	P37	9	10	N38	N_6
P_5	R37	11	12	P38	P_6
N_7	M39	13	14	L39	N_8
P_7	N39	15	16	M38	P_8
P_9	K38	17	18	K40	P_10
N_9	J38	19	20	K39	N_10
N_11	U38	21	22	W38	N_12
P_11	T37	23	24	V39	P_12
N_13	AA36	25	26	AA34	P_14
P_13	AA35	27	28	Y34	N_14
N_15	W35	29	30	W36	P_16
P_15	Y35	31	32	W37	N_16
N_17	G42	33	34	G41	N_18
P_17	F42	35	36	F41	P_18
S_1	R39	37	38	H40	CLK0
+3.3V	H39	39	40	J40	CLK1
+3.3V	H38	41	42		XRM_SERID
+3.3V	F40	43	44		RESERVED
+5V	F39	45	46		XRM_VREF
+5V	P37	47	48		XRM_VCCIO
VBAT	R37	49	50		XRM_VCCIO
+12V	M39	51	52		XRM_VCCIO
+12V	N39	53	54		-12V
PRESENCE_L	K38	55	56		XRM_TDI
XRM_TCK	J38	57	58		XRM_TRST
XRM_TMS	U38	59	60		XRM_TDO

Table 8 XRM Interface - part 1

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
N_19	J41	61	62	K42	N_20
P_19	H41	63	64	J42	P_20
N_21	M41	65	66	N41	N_22
P_21	L42	67	68	M42	P_22
N_23	P40	69	70	Y40	N_24
P_23	N40	71	72	W40	P_24
N_25	AA39	73	74	Y37	P_26
P_25	AA40	75	76	AA37	N_26
P_27	P41	77	78	U41	N_28
N_27	R40	79	80	T42	P_28
N_29	V41	81	82	V40	P_30
P_29	U42	83	84	W41	N_30
N_31	Y42	85	86	AA41	N_32
P_31	W42	87	88	AA42	P_32
CLK2	Y39	89	90	T40	S_4
CLK3	Y38	91	92	AF40	S_5
S_2	T39	93	94	AL42	S_6
S_3	L40	95	96	AE37	S_7
CLK4	AE40	97	98	AD42	N_34
CLK5	AD40	99	100	AC41	P_34
N_33	AB42	101	102	AV40	CLK6
P_33	AB41	103	104	AU39	CLK7
S_8	AK38	105	106	AH39	S_10
S_9	AG39	107	108		XRM_CLKIN_N
XRM_MGTREF_P		109	110		XRM_CLKIN_P
XRM_MGTREF_N		111	112		XRM_SDA
XRM_PECL_N		113	114		XRM_SCL
XRM_PECL_P		115	116		RESERVED
XRM_TX7_P		117	118		XRM_RX7_P
XRM_TX7_N		119	120		XRM_RX7_N

Table 9 XRM Interface - part 2

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
P_35	AE42	121	122	AF41	P_36
N_35	AD41	123	124	AF42	N_36
N_37	AH41	125	126	AJ42	P_38
P_37	AG42	127	128	AJ41	N_38
P_39	AH40	129	130	AB37	P_40
N_39	AJ40	131	132	AB38	N_40
N_41	AC38	133	134	AC39	N_42
P_41	AB39	135	136	AC40	P_42
P_43	AL41	137	138	AN41	N_44
N_43	AK42	139	140	AM41	P_44
P_45	AP42	141	142	AT42	N_46
N_45	AP41	143	144	AR42	P_46
N_47	AU41	145	146	AC35	P_50
P_47	AT41	147	148	AB36	N_50
P_49	AB34	149	150	AV41	N_48
N_49	AC34	151	152	AU42	P_48
P_51	AC36	153	154	AD37	N_52
N_51	AD35	155	156	AD36	P_52
N_53	AE38	157	158	AG38	N_54
P_53	AE39	159	160	AF39	P_54
P_55	AG37	161	162	AP40	N_56
N_55	AF37	163	164	AN40	P_56
N_57	AT40	165	166	AR39	N_58
P_57	AR40	167	168	AT39	P_58
N_59	AK39	169	170	AH38	N_60
P_59	AJ38	171	172	AJ37	P_60
N_61	AM39	173	174	AP38	N_62
P_61	AL39	175	176	AN39	P_62
N_63	AM38	177	178	AL37	N_64
P_63	AN38	179	180	AM37	P_64

Table 10 XRM Interface - part 3

4.7.3. XRM Interface – MGT Links

Eight lanes of user MGT (GTP) links are routed to the XRM interface. Lanes 0 – 6 are routed through Samtec QSE-DP connector, CN2. Lane 7 is routed through the Samtec QSH connector, CN1.

Signal	FPGA Pin	GTP Number	Samtec Pin
XRM_TX0_P	AA2	112B	1
XRM_TX0_N	Y2	“	3
XRM_RX0_P	Y1	“	2
XRM_RX0_N	W1	“	4
XRM_TX1_P	T2	112A	5
XRM_TX1_N	U2	“	7
XRM_RX1_P	U1	“	6
XRM_RX1_N	V1	“	8
XRM_TX2_P	R2	116B	17
XRM_TX2_N	P2	“	19
XRM_RX2_P	P1	“	18
XRM_RX2_N	N1	“	20
XRM_TX3_P	K2	116A	21
XRM_TX3_N	L2	“	23
XRM_RX3_P	L1	“	22
XRM_RX3_N	M1	“	24
XRM_TX4_P	J2	120B	9
XRM_TX4_N	H2	“	11
XRM_RX4_P	H1	“	10
XRM_RX4_N	G1	“	12
XRM_TX5_P	D2	120A	13
XRM_TX5_N	E2	“	15
XRM_RX5_P	E1	“	14
XRM_RX5_N	F1	“	16
XRM_TX6_P	B1	124B	25
XRM_TX6_N	B2	“	27
XRM_RX6_P	A2	“	26
XRM_RX6_N	A3	“	28
XRM_TX7_P	B6	124A	(CN1) 117
XRM_TX7_N	B5	“	(CN1) 119
XRM_RX7_P	A5	“	(CN1) 118
XRM_RX7_N	A4	“	(CN1) 120

Table 11 XRM Interface - MGT Links

4.8. Pn4 I/O

Up to 3 pairs of differential or 6 single-ended signals are available on Pn4 and are sourced from Bank 10 of the User FPGA. All of the signal traces are routed as 100 Ohm differential pairs and each pair is matched in length. The worst case difference in trace length between any two pairs is 10mm.

Signal	FPGA Pin	Pn4 Pin	Pn4 Pin	FPGA Pin	Signal
PN4_P1	AK12	1 [CC]	2 [CC]	AJ30	PN4_P2
PN4_N1	AK13	3 [CC]	4 [CC]	AK30	PN4_N2
PN4_P3	AM28	5	6	-	-
PN4_N3	AL29	7	8	-	-
-	-	9	10	-	-
-	-	11	12	-	-
-	-	13	14	-	-
-	-	15	16	-	-
-	-	17	18	-	-
-	-	19	20	-	-
-	-	21	22	-	-
-	-	23	24	-	-
-	-	25	26	-	-
-	-	27	28	-	-
-	-	29	30	-	-
-	-	31	32	-	-
-	-	33	34	-	-
-	-	35	36	-	-
-	-	37	38	-	-
-	-	39	40	-	-
-	-	41	42	-	-
-	-	43	44	-	-
-	-	45	46	-	-
-	-	47	48	-	-
-	-	49	50	-	-
-	-	51	52	-	-
-	-	53	54	-	-
-	-	55	56	-	-
-	-	57	58	-	-
-	-	59	60	-	-
-	-	61	62	-	-
-	-	63	64	-	-

Table 12 Pn4 to FPGA Assignments

In Table 12, pins marked [CC] are clock capable and may be used to access the regional clocking resources in the FPGA.

4.8.1. Pn4 Signalling Voltage

The signalling voltage on the Pn4 is fixed at 3.3V

4.9. XMC Interface

4.9.1. Primary XMC Connector, P15

The MGT (GTP) links connected between the user FPGA and the Primary XMC connector, P15, are compatible with PCI Express and Serial RapidIO. Depending upon the carrier card, they may also be used for user-specific applications.

Signal	FPGA Pin	GTP Number	P15 Pin
PCIE_TX0_P	AB2	114A	A1
PCIE_TX0_N	AC2	"	B1
PCIE_RX0_P	AC1	"	A11
PCIE_RX0_N	AD1	"	B11
PCIE_TX1_P	AG2	114B	D1
PCIE_TX1_N	AF2	"	E1
PCIE_RX1_P	AF1	"	D11
PCIE_RX1_N	AE1	"	E11
PCIE_TX2_P	AH2	118A	A3
PCIE_TX2_N	AJ2	"	B3
PCIE_RX2_P	AJ1	"	A13
PCIE_RX2_N	AK1	"	B13
PCIE_TX3_P	AN2	118B	D3
PCIE_TX3_N	AM2	"	E3
PCIE_RX3_P	AM1	"	D13
PCIE_RX3_N	AL1	"	E13
PCIE_TX4_P	AP2	122A	A5
PCIE_TX4_N	AR2	"	B5
PCIE_RX4_P	AR1	"	A15
PCIE_RX4_N	AT1	"	B15
PCIE_TX5_P	AW2	122B	D5
PCIE_TX5_N	AV2	"	E5
PCIE_RX5_P	AV1	"	D15
PCIE_RX5_N	AU1	"	E15
PCIE_TX6_P	BA1	126A	A7
PCIE_TX6_N	BA2	"	B7
PCIE_RX6_P	BB2	"	A17
PCIE_RX6_N	BB3	"	B17
PCIE_TX7_P	BA6	126B	D7
PCIE_TX7_N	BA5	"	E7
PCIE_RX7_P	BB5	"	D17
PCIE_RX7_N	BB4	"	E17

Table 13 XMC P15 Connections

4.10. XRM IO146 Interface

The following tables provide the user with information on the pin-out of the XRM-IO146 when fitted to an ADM-XRC-5TZ version card.

The signal names P_1/N_1 etc are internal to the ADM-XRC-5TZ. The important mapping is between the Mictor pin and the FPGA pin.

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_1	H38	3	1	2	6	E39	P_4
N_1	H39	1	3	4	8	E40	N_4
P_3	F39	7	5	6	4	G38	P_2
N_3	F40	5	7	8	2	G39	N_2
P_5	R37	11	9	10	12	P38	P_6
N_5	P37	9	11	12	10	N38	N_6
P_7	N39	15	13	14	16	M38	P_8
N_7	M39	13	15	16	14	L39	N_8
P_9	K38	17	17	18	18	K40	P_10
N_9	J38	19	19	20	20	K39	N_10
P_11	T37	23	21	22	24	V39	P_12
N_11	U38	21	23	24	22	W38	N_12
P_13	AA35	27	25	26	26	AA34	P_14
N_13	AA36	25	27	28	28	Y34	N_14
P_15	Y35	31	29	30	30	W36	P_16
N_15	W35	29	31	32	32	W37	N_16
S_1	R39	37	33	34	38	H40	CLK0
S_2	T39	93	35	36	40	J40	CLK1
+5V		-	37	38	90	T40	S_4

Table 14 IO146 Mictor Connector Pins 1 - 38

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_17	F42	35	39	40	36	F41	P_18
N_17	G42	33	41	42	34	G41	N_18
P_19	H41	63	43	44	64	J42	P_20
N_19	J41	61	45	46	62	K42	N_20
P_21	L42	67	47	48	68	M42	P_22
N_21	M41	65	49	50	66	N41	N_22
P_23	N40	71	51	52	72	W40	P_24
N_23	P40	69	53	54	70	Y40	N_24
P_25	AA40	75	55	56	74	Y37	P_26
N_25	AA39	73	57	58	76	AA37	N_26
P_27	P41	77	59	60	80	T42	P_28
N_27	R40	79	61	62	78	U41	N_28
P_29	U42	83	63	64	82	V40	P_30
N_29	V41	81	65	66	84	W41	N_30
P_31	W42	87	67	68	88	AA42	P_32
N_31	Y42	85	69	70	86	AA41	N_32
S_8	AK38	105	71	72	89	Y39	CLK2
S_9	AG39	107	73	74	91	Y38	CLK3
+5V		-	75	76	95	L40	S_3

Table 15 IO146 Mictor Connector Pins 39 - 76

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_33	AB41	103	77	78	100	AC41	P_34
N_33	AB42	101	79	80	98	AD42	N_34
P_35	AE42	121	81	82	122	AF41	P_36
N_35	AD41	123	83	84	124	AF42	N_36
P_37	AG42	127	85	86	126	AJ42	P_38
N_37	AH41	125	87	88	128	AJ41	N_38
P_39	AH40	129	89	90	130	AB37	P_40
N_39	AJ40	131	91	92	132	AB38	N_40
P_41	AB39	135	93	94	136	AC40	P_42
N_41	AC38	133	95	96	134	AC39	N_42
P_43	AL41	137	97	98	140	AM41	P_44
N_43	AK42	139	99	100	138	AN41	N_44
P_45	AP42	141	101	102	144	AR42	P_46
N_45	AP41	143	103	104	142	AT42	N_46
P_47	AT41	147	105	106	152	AU42	P_48
N_47	AU41	145	107	108	150	AV41	N_48
S_5	AF40	92	109	110	97	AE40	CLK4
S_6	AL42	94	111	112	99	AD40	CLK5
+5V		-	113	114	-		+5V

Table 16 IO146 Mictor Connector Pins 77 – 114

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_49	AB34	149	115	116	146	AC35	P_50
N_49	AC34	151	117	118	148	AB36	N_50
P_51	AC36	153	119	120	156	AD36	P_52
N_51	AD35	155	121	122	154	AD37	N_52
P_53	AE39	159	123	124	160	AF39	P_54
N_53	AE38	157	125	126	158	AG38	N_54
P_55	AG37	161	127	128	164	AN40	P_56
N_55	AF37	163	129	130	162	AP40	N_56
P_57	AR40	167	131	132	168	AT39	P_58
N_57	AT40	165	133	134	166	AR39	N_58
P_59	AJ38	171	135	136	172	AJ37	P_60
N_59	AK39	169	137	138	170	AH38	N_60
P_61	AL39	175	139	140	176	AN39	P_62
N_61	AM39	173	141	142	174	AP38	N_62
P_63	AN38	179	143	144	180	AM37	P_64
N_63	AM38	177	145	146	178	AL37	N_64
S_7	AE37	96	147	148	102	AV40	CLK6
S_10	AH39	106	149	150	104	AU39	CLK7
+5V		-	151	152	-		+5V

Table 17 IO146 Mictor Connector Pins 115 - 152

5. XRM HSSDC2A Interface

Signal	FPGA Pin	GTP Number	Samtec Pin	XRM Pin
XRM_TX0_P	AA2	112B	CN2-1	**P1-6**
XRM_TX0_N	Y2	“	CN2-3	**P1-5**
XRM_TX1_P	T2	112A	CN2-5	**P2-6**
XRM_TX1_N	U2	“	CN2-7	**P2-5**
XRM_TX2_P	R2	116B	CN2-17	**P3-6**
XRM_TX2_N	P2	“	CN2-19	**P3-5**
XRM_TX3_P	K2	116A	CN2-21	**P4-6**
XRM_TX3_N	L2	“	CN2-23	**P4-5**
XRM_RX0_P	Y1	112B	CN2-2	**P1-2**
XRM_RX0_N	W1	“	CN2-4	**P1-3**
XRM_RX1_P	U1	112A	CN2-6	**P2-2**
XRM_RX1_N	V1	“	CN2-8	**P2-3**
XRM_RX2_P	P1	116B	CN2-18	**P3-2**
XRM_RX2_N	N1	“	CN2-20	**P3-3**
XRM_RX3_P	L1	116A	CN2-22	**P4-2**
XRM_RX3_N	M1	“	CN2-24	**P4-3**

Table 18 XRM-HSSDC2A-5T2 Pinout

6. Revision History

Date	Revision	Nature of Change
18-07-2008	1.0	Initial release.
04-08-2008	1.1	Modified SysMon voltage description for PCI VIO (+3V0)
13-08-2008	1.2	Removed references to XRC-5T2, updated description for MCLK usage.
31-08-2009	2.0	1.1: Added Front I/O voltages, 2.2: Added note on power estimation and current requirements, 2.3: New section on PCI mode selection, 2.6: New section on cooling requirements, 4.2.1: Added diagram of flash organisation, 4.2.1.1: New section on power-up sequence, 4.2.1.2: New section on One-Time Configuration feature, 4.3.1: New section on Automatic Temperature Monitoring, 4.5.1: Added note on default LCLK rate, 4.5.3: Note on PCIe Clock availability, 4.5.4: Note on MGT clock defaults.