ALPHA DATA

# ADM-XRC-6TGE User Manual

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# Table Of Contents

# Tables

# Figures

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# 1 Introduction

The **ADM-XRC-6TGE** is a high-performance XMC for applications using Virtex-6 FPGAs from Xilinx. This card supports all Virtex-6 LXT and SXT devices available in the FF(G)1759 package.

The **ADM-XRC-6TGE** features a 10/100/1000Base-T Ethernet link to the target FPGA provided through the Pn6 interface.

The **ADM-XRC-6TGE** is targeted for use on 3U and 6U VPX carrier cards and its Rear I/O (Pn4 and Pn6) is compatible with various VITA 46.9 PMC/XMC to VPX signal mapping configurations.

The **ADM-XRC-6TGE** includes a separate FPGA with a PCIe bridge developed by Alpha Data. Using a separate device allows high performance operation without the need to integrate proprietary cores in the user (target) FPGA.

## 1.1 Key Features

**Key Features**

- Single-width XMC, compliant to VITA Standard 42.0 and 42.3
- Dedicated 4-lane PCI-Express Gen 2 interface with high-performance DMA controllers
- 4 additional GTX links between user FPGA and P5
- Support for Virtex-6 FPGA in FF(G)1759 package
- 4 independent banks of DDR3-800 SDRAM, 256MB/bank, 1GB total (2GB option)
- Front-panel (XRM) interface with adjustable voltage, 146 GPIO signals and 8 GTX links to user FPGA
- Rear-panel (XMC) interface with a 10/100/1000Base-T Ethernet link, 4 GTX links & 44 GPIO signals between user FPGA and P6
- Rear-panel (PMC) interface with 64 GPIO signals between user FPGA and P4 (optional)
- Rear-Panel I/O (Pn6 and Pn4) compatible with 3U and 6U VPX carriers featuring various VITA 46.9 PMC/XMC to VPX signal mapping configurations
- On-board programmable clocks enabling multiple protocols to be implemented on the user FPGA's high-speed links
- Voltage and temperature monitoring
- Air-cooled and conduction-cooled configurations

## 1.2 References & Specifications

| | |
|---|---|
| ANSI/VITA 42.0 | *XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3 |
| ANSI/VITA 42.3 | *XMC PCI Express Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4 |
| ANSI/VITA 46.9 | *PMC/MXC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard*, November 2010, VITA, ISBN 1-885731-63-9 |
| ANSI/IEEE 1386-2001 | *IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5 |
| ANSI/IEEE 1386.1-2001 | *IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7 |
| ANSI/VITA 20-2001 (R2005) | *Conduction Cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4 |

**Table 1: References**

# 2 Installation

## 2.1 Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

## 2.2 Hardware Installation

### 2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

### 2.2.2 Motherboard / Carrier Requirements

The **ADM-XRC-6TGE** is a single width XMC.3 mezzanine with optional P6 and P4 connectors. The motherboard/ carrier must comply with the XMC.3 (VITA 42.3) specification for the Primary XMC connector, J5.

The Secondary XMC connector, P6 has a pinout compatible with various XMC to VPX signal maps as defined by VITA 46.9. In particular the the Gigabit Ethernet interface is part of the VITA 46.9 X12d signal group, making it accessible on most VPX carriers. Please consult the pinouts in this user-guide as-well as those of the carrier manufacturer prior to installation. Assistance can be provided by Alpa Data.

> **IMPORTANT:** Connector P6 on the card is not compatible with the VITA 42.10 (XMC GPIO) Standard. In particular, USB VCC must not be applied on this connector.

The **ADM-XRC-6TGE** is compatible with either 5V or 12V on the "VPWR" power rail.

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact current requirements for each power rail.

# 3 Functional Description

## 3.1 Overview

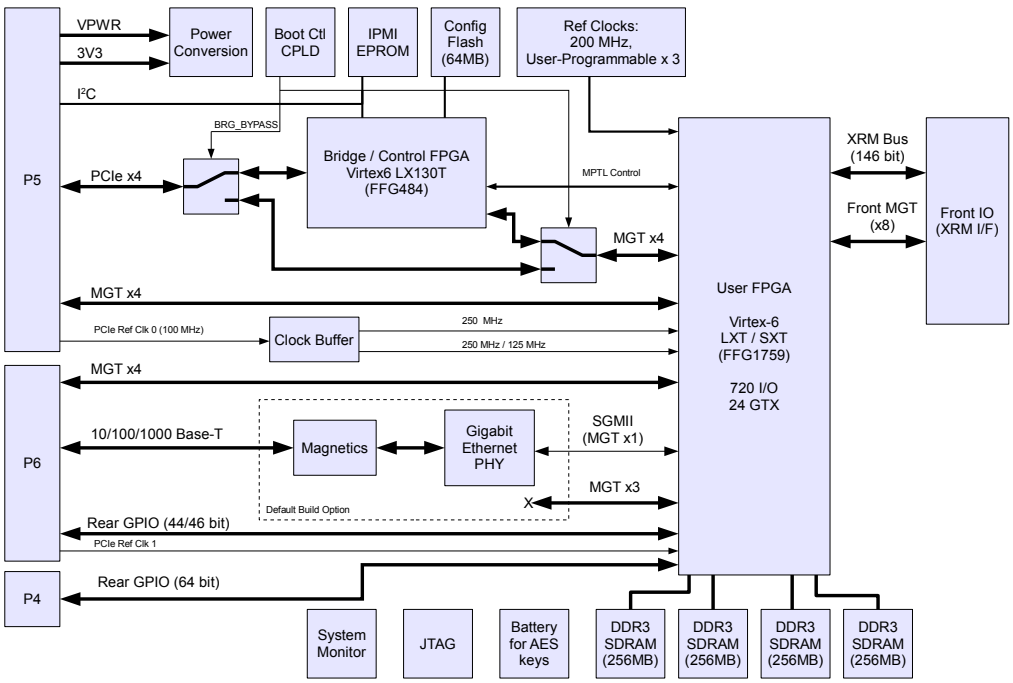



**Figure 1: ADM-XRC-6TGE Block Diagram**

### 3.1.1 Switch Definitions

There is a set of eight DIP switches placed on the rear of the board. Their functions are described in **Table 2 'Switch Definitions'**.

> **Note:** With the exception of SW1-8 which enables the 125 MHz clock for use with the Ethernet interface, all switches are OFF by default. *Factory Test* and *Reserved* switches must be in the OFF position for normal operation.

| Switch Ref. | Function | ON State | Off State |
|---|---|---|---|
| SW1-1 | Bridge Bypass | Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the user FPGA. | Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge. |
| SW1-2 | *Factory Test* | Factory Test Mode | Normal Operation |
| SW1-3 | E-Fuse | Enable E-Fuse programming voltage (VccEFuse = 2.5V) | Disable E-Fuse programming voltage (VccEFuse = 0V) |
| SW1-4 | XMC JTAG | Connect JTAG chain to P5 | Isolate JTAG chain from P5 |
| SW1-5 | *Reserved* | - | - |
| SW1-6 | Flash Boot Inhibit | Target FPGA is not configured from onboard flash memory. | Target FPGA is configured from on-board flash memory. |
| SW1-7 | *Reserved* | - | - |
| SW1-8 | 125 MHz PCIe Ref Clock | Clock input to Target FPGA GTX Quad 112 is 125 MHz | Clock input to Target FPGA GTX Quad 112 is 250 MHz |

**Table 2: Switch Definitions**

## 3.1.2 LED Definitions

The position and description of the board status LEDs are shown in **Figure 2, "LED Positions"**:

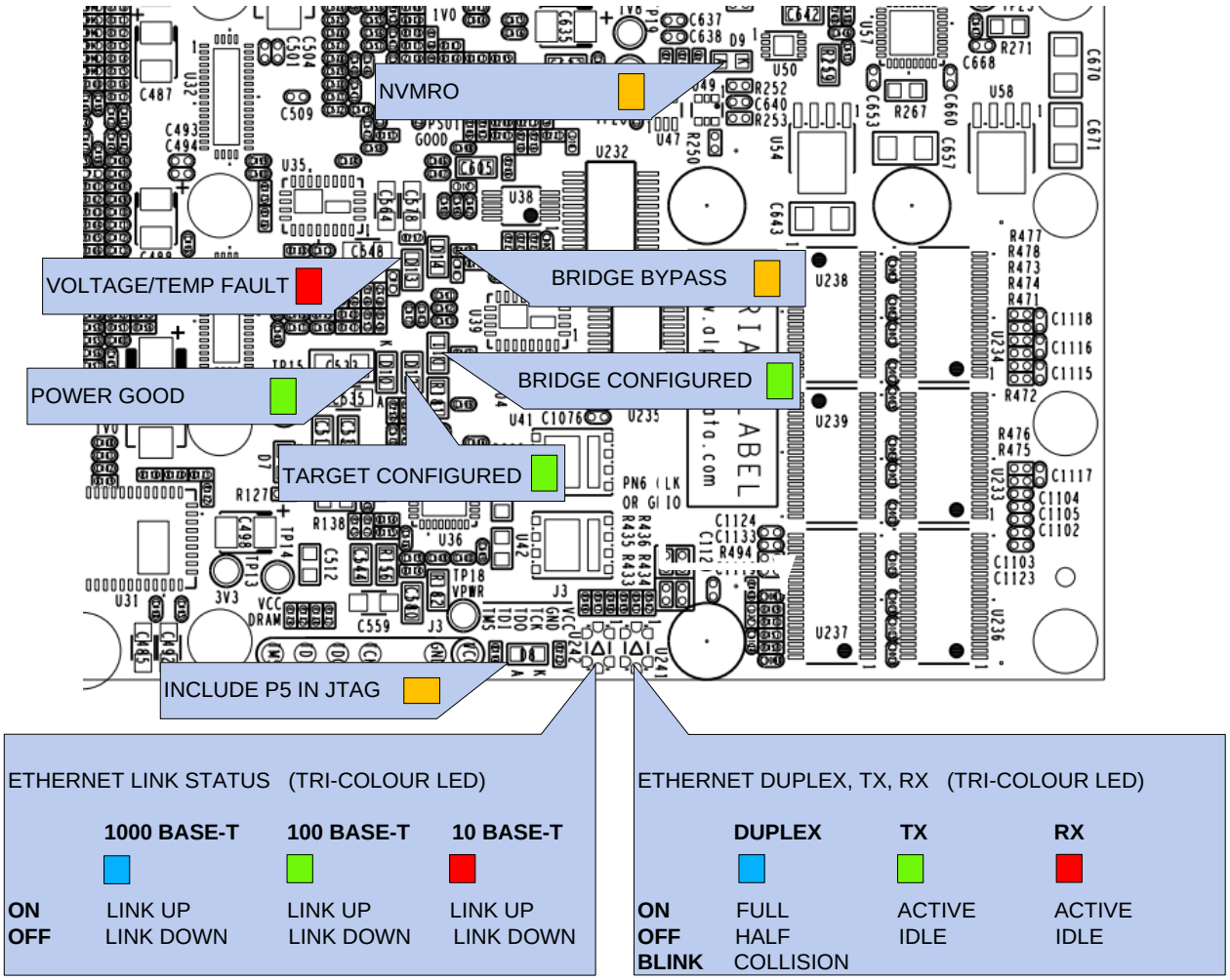



**Figure 2: LED Positions**

## 3.2 XMC Platform Interface

### 3.2.1 IPMI I2C

A 4 Kbit I2C EEPROM (type M24C04) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

### 3.2.2 MBIST#

Built-In Self Test. This output signal is driven active (low) until the FPGA with PCIe interface is configured. In normal operation, this is the bridge FPGA. In Bridge Bypass mode, it is the target FPGA.

### 3.2.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D7.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the target FPGA at pin AD30.

### 3.2.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier. When asserted, the bridge FPGA will be reset.

The MRSTI# signal is translated to 2.5V levels and connected to the target FPGA at pin AC30.

### 3.2.5 MRSTO#

XMC Reset Out. This optional output signal is unused and undriven.

### 3.2.6 MPRESENT#

Module Present. This output signal is connected directly to 0V.

# 3.3 JTAG Interface

## 3.3.1 On-board Interface

A JTAG boundary scan chain is connected to header J3. This allows the connection of the Xilinx JTAG cable for FPGA debug using the Xilinx ChipScope tools.

The JTAG Header pinout is shown in **Figure 3, "JTAG Header J2"**:

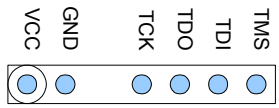



**Figure 3: JTAG Header J2**

The scan chain is shown in **Figure 4, "JTAG Boundary Scan Chain"**:

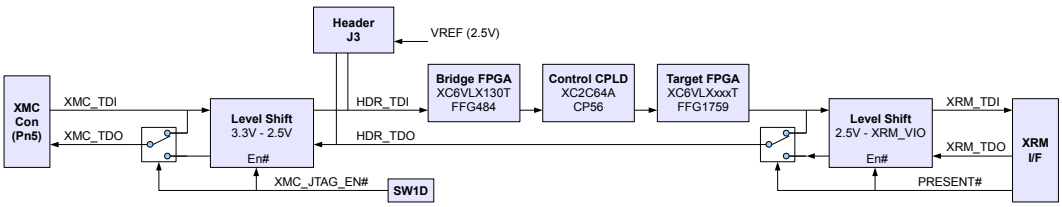



**Figure 4: JTAG Boundary Scan Chain**

If the boundary scan chain is connected to the interface at the XMC connector (SW1-4 is ON), Header J3 should not be used.

## 3.3.2 XMC Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The interface can be connected to the on-board interface (through level-translators) by switching SW1-4 ON. See **Section 3.1.1, "Switch Definitions"**

## 3.3.3 JTAG Voltages

The on-board JTAG scan chain uses 2.5V. The Vcc supply provided on J3 to the JTAG cable is +2.5V and is protected by a poly fuse rated at 350mA. 3.3V signals must not be used at header J3.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the XRM interface use the adjustable voltage XRM_VIO.

## 3.4 Clocks

The **ADM-XRC-6TGE** provides a wide variety of clocking options. On top of a fixed 200MHz oscillator and clocks routed from the rear and front panel connectors, the board has 3 user-programmable clocks. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

A complete overview of the clock routing on the **ADM-XRC-6TGE** is given in **Figure 5, "Clocks"**. A description of each clock follows.

> **Note:** Clock Termination
> The LVDS clocks do not have termination resistors on the circuit board. On-die terminations in the FPGA must be enabled by setting the attribute "DIFF_TERM = TRUE". This can either be set in the source code when instantiating the buffer, or in the User Constraints File (UCF). See the Xilinx Virtex-6 Libraries Guide and Constraints Guide for further details.

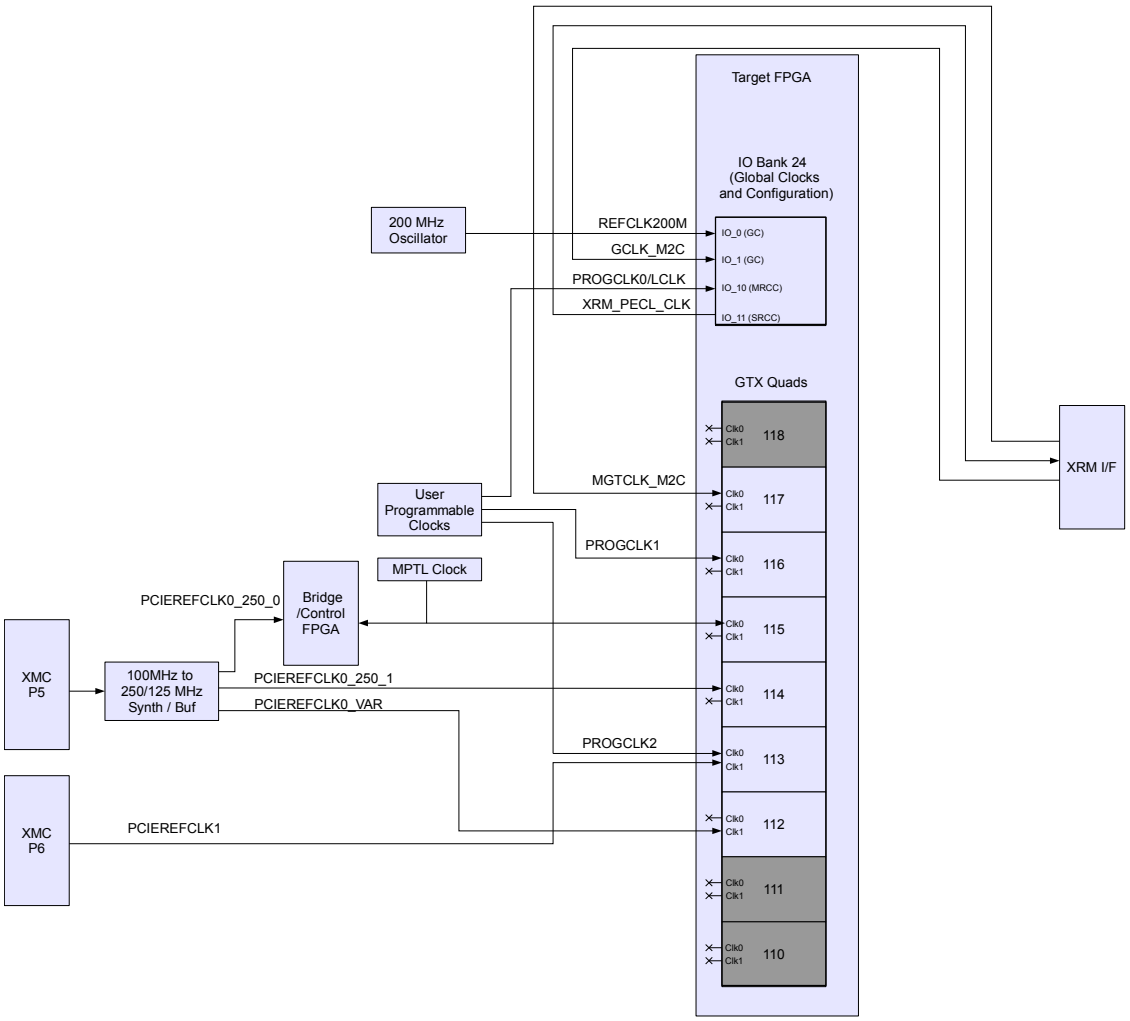



**Figure 5: Clocks**

### 3.4.1 200MHz Reference Clock (REFCLK200M)

The fixed 200MHz reference clock REFCLK200M is a differential clock signal using LVDS. It is connected to a Global Clock input on the Target FPGA at pins AE30 and AF30.

This clock can be used to generate application-specific clock frequencies using the PLLs within the Virtex-6 FPGA. It is also suitable as the reference clock for the IO delay control block (IDELAYCTRL).

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| REFCLK200M | 200 MHz | IO_L0_GC_24 | LVDS_25 | AE30 | AF30 |

**Table 3: REFCLK200M Connections**

### 3.4.2 PCIe Reference Clock 0 (PCIEREFCLK0)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector, P5 at pins A19 and B19. Three clocks are derived from this reference clock: a 250 MHz clock to the Bridge FPGA, a 250 MHz clock to the Target FPGA at GTX Quad 114 and a further clock to the Target FPGA at GTX Quad 112 which is configurable between 250 MHz and 125 MHz. The selection between 250 MHz and 125 MHz is made by switch SW1-8 as described in **Table 2 'Switch Definitions'**.

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| PCIEREFCLK0_250_1 | 250 MHz | MGTREFCLK1_114 | LVDS_25 | AB8 | AB7 |
| PCIEREFCLK0_VAR | 250/125 MHz | MGTREFCLK0_112 | LVDS_25 | AH8 | AH7 |

**Table 4: PCIEREFCLK0 Connections**

### 3.4.3 PCIe Reference Clock 1 (PCIEREFCLK1)

The reference clock "PCIEREFCLK1" is a differential clock provided by a carrier card through the Secondary XMC connector P6 at pins A19 and B19. This clock is connected straight to the Target FPGA at GTX Quad 113. It may be used as part of a secondary PCIe interface at P6. If P6 forms part of the primary PCIe interface, PCIEREFCLK0 is used, not this clock.

The use of P6 pins A19 and B19 as a reference clock is the default factory build option. Please consult the online order code generator for configuring these pins as general purpose IO or contact Alpha Data directly.

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| PCIEREFCLK1 | Direct from Carrier | MGTREFCLK1_113 | LVDS_25 | AD8 | AD7 |

**Table 5: PCIEREFCLK1 Connections**

### 3.4.4 Programmable Clocks (PROGCLK 0-2)

There are three user-programmable differential clocks using LVDS. These clocks are programmable through the Alpha Data ADM-XRC Gen 3 SDK. PROGCLK0 is generated in the Bridge FPGA by the the Alpha Data ADB3 driver and offers a less accurate frequency resolution, but with a wider programmable frequency range. PROGCLK1 and PROGCLK2 are generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments).

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| LCLK/PROGCLK0 | 5 - 700 MHz | IO_L10_MRCC_24 | LVDS_25 | AA31 | AB31 |
| PROGCLK1 | 5 - 312.5 MHz | MGTREFCLK0_116 | LVDS_25 | M8 | M7 |
| PROGCLK2 | 5 - 312.5 MHz | MGTREFCLK0_113 | LVDS_25 | AF8 | AF7 |

**Table 6: PROGCLK Connections**

### 3.4.5 Module-Carrier Global Clock (GCLK_M2C)

The clock "GCLK_M2C" is a differential clock signal using LVDS. It is provided by an XRM module through the XRM connector, CN1, at pins 110 & 108. It is connected to a Global Clock input on the Target FPGA.

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| GCLK_M2C | Variable | IO_L1_GC_24 | LVDS_25 | W30 | V30 |

**Table 7: GCLK_M2C Connections**

### 3.4.6 Module-Carrier MGT Clock (MGTCLK_M2C)

The reference clock "MGTCLK_M2C" is a differential clock signal using LVDS. The clock is provided by an XRM module through the XRM connector, CN1, at pins 109 & 111. It is connected to GTX Quad 117 on the Target FPGA for application specific frequencies / line rates.

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| MGTCLK_M2C | Variable | MGTREFCLK0_117 | LVDS_25 | G10 | G9 |

**Table 8: MGTCLK_M2C Connections**

### 3.4.7 XRM PECL Clock (XRM_PECL_CLK)

The clock "XRM_PECL_CLK" is a differential clock signal using 2.5V PECL levels. The clock is provided by the target FPGA and connected to an XRM module through the XRM connector, CN1, at pins 113 & 115.

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| XRM_PECL_CLK | Variable | IO_L11_MRCC_24 | LPECL_25 | R32 | T32 |

**Table 9: XRM_PECL_CLK Connections**

# 3.5 Flash Memory

A 512Mb Flash Memory (Intel / Numonyx PC28F512P30EF) is used to store board Vital Product Data (VPD), programmable clock parameters and configuration bitstreams for the Bridge and Target FPGAs.

The flash memory cannot be accessed by the target FPGA. Host access is only possible through the FLCTL, FLPAGE and FLDATA registers in the Bridge FPGA.

The region of memory between addresses 0x11000000 and 0x11FFFFF is allocated for custom data to be stored by the **ADM-XRC-6TGE** user.

Utilities for erasing, programming and verification of the flash memory are provided in the ADMXRC SDK.

**Write Protect**

The Flash Write Protect (WP#) pin is connected to an inverted version of the NVMRO signal at the XMC interface. When the NVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED as shown in **Figure 2, "LED Positions"**.

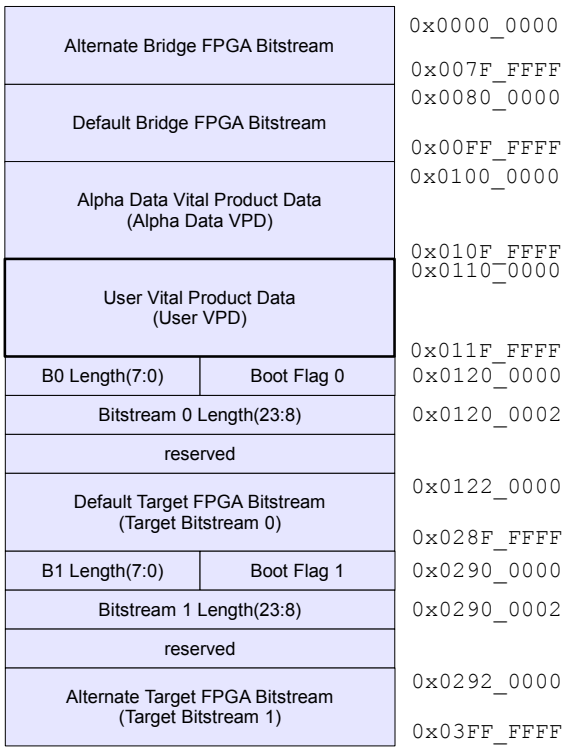



**Figure 6: Flash Memory Map**

# 3.6 Configuration

## 3.6.1 Power-Up Sequence

If valid data is stored in the flash memory, the bridge will automatically set the programmable clock generator and configure the Target FPGA at power-up.

This sequence can be inhibited by turning the Flash Boot Inhibit (FBI) switch, SW1-6 to ON. (See **Table 2 'Switch Definitions'**).

> **Note:** If an over-temperature alert is detected from the System Monitor, the target **will be cleared** by pulsing its PROG signal. See **Section 3.7.1, "Automatic Temperature Monitoring"**.

## 3.7 Health Monitoring

The **ADM-XRC-6TGE** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Xilinx System Monitor (XSM) core within the Bridge FPGA and a National Semiconductor LM87 located on the board.

Control logic within the Bridge FPGA automatically scans the XSM and LM87 once per second and stores the current measurements in blockram.

The following voltage rails and temperatures are monitored:

| **Monitor** | *Purpose* |
|---|---|
| 1.0V | FPGA Core Supply (VccINT) |
| 1.5V | DDR3 SDRAM, Target FPGA memory I/O |
| 1.8V | Flash Memory, DC-DC converters for GTX Supplies |
| 2.5V | FPGA Auxiliary Supply (VccAUX) |
| XRM_VIO | (Front-Panel) I/O voltage |
| 3.3V | Board Input Supply |
| 5.0V | Internally generated 5V supply |
| VPWR | Board Input Supply (either 5.0V or 12.0V) |
| Temp1 | Target FPGA on-die temperature |
| Temp2 | LM87 on-die temperature |
| Temp3 | Bridge FPGA on-die temperature |
| Brg 1.0V | Bridge FPGA Core Supply (VccINT) |
| Brg 2.5V | Bridge FPGA Auxiliary Supply (VccAUX) |

**Table 10: Voltage and Temperature Monitors**

An example application that reads the system monitor ("sysmon") is available within the SDK.

### 3.7.1 Automatic Temperature Monitoring

At power-up, the control logic sets the temperature limits and resets the LM87's over-temperature interrupt.

The temperature limits are shown in **Table 11 'Temperature Limits'**:

| | Target FPGA | | Board (LM87) | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| Commercial | 0°C | +85°C | 0°C | +70°C |
| Extended | 0°C | +100°C | 0°C | +85°C |
| Industrial | -40°C | +100°C | -40°C | +85°C |

**Table 11: Temperature Limits**

**Important:**

If any temperature limit is exceeded, the Target FPGA is automatically cleared. This is indicated by the Green LED (Target Configured) switching off and the Red LED(Voltage/TempFault) switching on.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

## 3.8 Local Bus

A Multiplexed Packet Transport Link (MPTL) connects the Bridge and Target FPGAs. It is capable of transferring data at up to 2GB/s simultaneously in each direction.

The MPTL replaces the parallel local bus used in previous generations of the ADM-XRC series. Details of the link and example designs are given in the Software Development Kit (SDK).

# 3.9 Target FPGA

## 3.9.1 I/O Bank Voltages

The Target FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in **Table 12 'Target FPGA IO Banks'**. Full details of the IOSTANDARD required for each signal are given in the SDK.

| IO Banks | Voltage | Purpose |
|---|---|---|
| 0, 24 | 2.5V | Configuration, JTAG, LBus Control,XMC Control,Target SelectMap Interface |
| 33,34 | 2.5V | Pn4 & Pn6 GPIO |
| 35 | 2.5V | Pn6 GPIO |
| 37, 36, 26, 25 | 1.5V | DRAM Banks 0 & 1 |
| 27 | 1.5V | DRAM Bank 0 |
| 13, 12 | 1.5V | DRAM Bank 2 |
| 23, 32, 22 | 1.5V | DRAM Banks 2 & 3 |
| 14, 15, 16, 17 | XRM_VIO | XRM Interface (variable voltage) |
| 21, 28, 38 | 1.5V | reserved |

**Table 12: Target FPGA IO Banks**

## 3.9.2 Target MGT Links

There are a total of 24 Multi-Gigabit Transceiver (MGT) links connected to the Target FPGA:

| Links | Width | Connection |
|---|---|---|
| RearMGT(3:0) | 4 | Bridge FPGA (for MPTL) or XMC Connector P5 lanes (3:0) in Bridge Bypass Mode |
| RearMGT(7:4) | 4 | Direct link to XMC P5 lanes (7:4) |
| RearMGT(11:8) | 4 | Direct link to XMC P6 lanes (3:0) |
| RearMGT(12) | 1 | Serial Link to Gigabit Ethernet PHY (If Ethernet link bypassed as build option: Direct link to XMC P6 lane (4)) |
| RearMGT(15:13) | 3 | RX half only provide direct link from XMC P6 lanes (7:5) (If Ethernet link bypassed as build option: Direct link to XMC P6 lanes (7:5)) |
| FrontMGT(7:0) | 8 | Direct link to XRM interface |

**Table 13: Target MGT Links**

The connections of these links are shown in **Figure 7, "MGT Links"**:

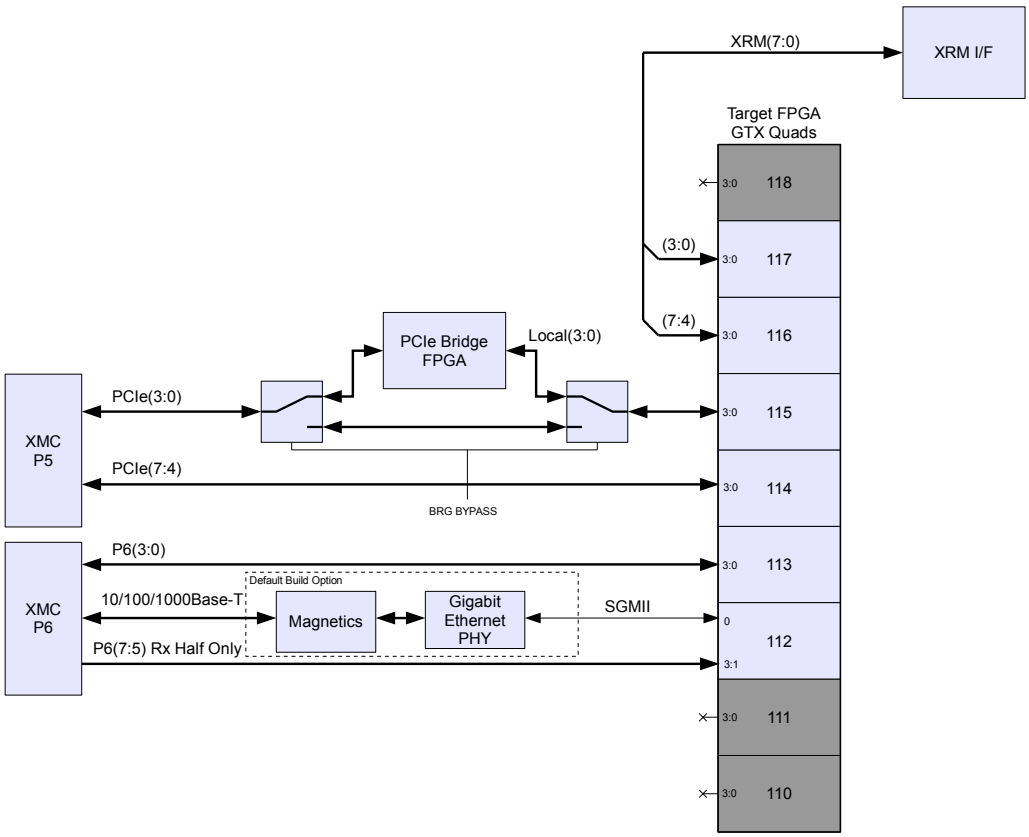



**Figure 7: MGT Links**

**Notes:**

(1) The numbering in the Target FPGA refers to the GTX Quad number. Each Quad contains a grouping of four **GTXE1** Multi-Gigabit Transceivers and two dedicated reference clock pairs.

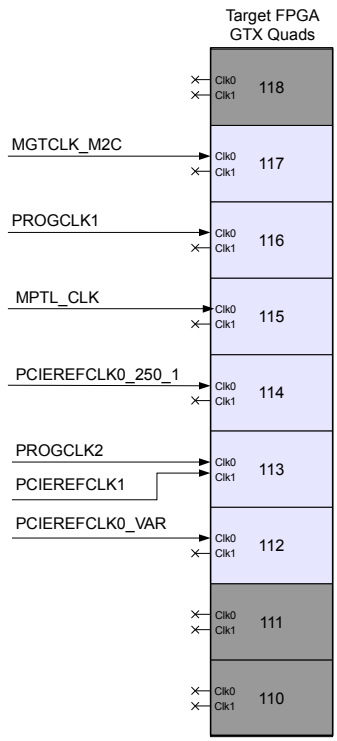



**Figure 8: MGT Clocks**

# 3.10 Gigabit Ethernet Link

The **ADM-XRC-6TGE** provides a complete Gigabit Ethernet hardware solution, enabling the on-board FPGA to directly communicate with a copper Ethernet network. The network interface to the Ethernet link is through 4 pin-pairs located on the secondary XMC connector, Pn6 which connect to the on-board PHY. A serial link is provided between the PHY and a GTX transceiver in the FPGA. The serial link is intended to be operated as a Serial Gigabit Media Independent Interface (SGMII) between the PHY and one of the FPGA's hard silicon Ethernet MACs.

The **ADM-XRC-6TGE** does not provide a functioning Ethernet link out-of-the-box: the user must instantiate a target FPGA design which uses one of the Ethernet MACs in the FPGA. In order to utilise the on-board PHY, the correct GTX transceiver must be constrained in the FPGA design. An overview of the Ethernet link including the user's FPGA design on the FPGA is shown in **Figure 9, "Gigabit Ethernet Link"**:

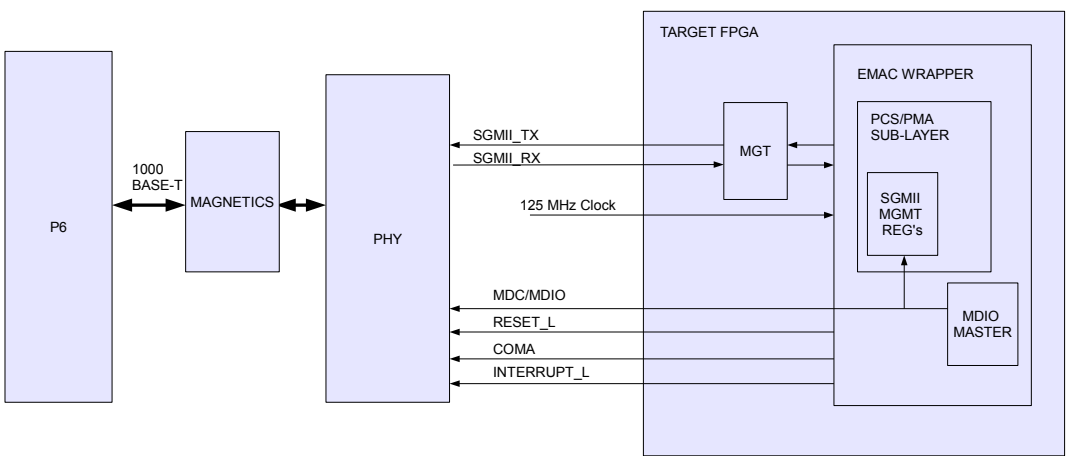



**Figure 9: Gigabit Ethernet Link**

### 3.10.1 Network Interface

**Appendix A2, "Secondary XMC Connector, P6"** illustrates the pin-out for the Ethernet link on XMC connector Pn6.

The **ADM-XRC-6TGE** is designed to be compatible with VITA 46 (VPX) modules with XMC mezzanine slots. VITA 46.9 is a standard which defines the mapping between XMC mezzanine connectors to the VPX connector wafers on VPX modules. The 4 pin-pairs comprising the Ethernet interface on the **ADM-XRC-6TGE** are part of the X12d pattern described in the VITA 46.9 documentation.

### 3.10.2 MAC Interface

The **ADM-XRC-6TGE** is designed to use one of the hard silicon TEMAC's in the Xilinx Virtex-6 FPGA. There is a serial link between a GTX quad on the FPGA and the PHY, on which an SGMII link can be implemented. The same GTX transceiver quad also has a high-quality 125 MHz clock input which is required for the SGMII link. The PCIe Reference Clock must be provided to the board and switch 1-8 must be in the ON position for this clock to present. Alternatively a programmable clock can be sourced from the GTX quad above.

For further information regarding the implementation of the SGMII link to the PHY, please consult Xilinx's *Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide* .

**Figure 10, "SGMII Interface at GTX Quad 112"** illustrates the connections to the GTX quad that provide the serial link to the PHY.

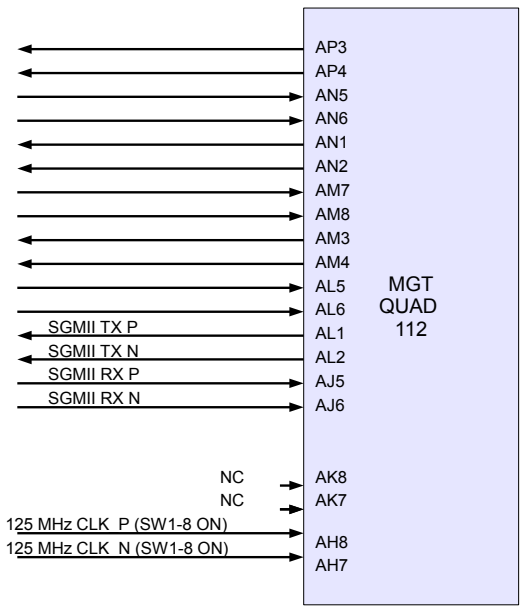



**Figure 10: SGMII Interface at GTX Quad 112**

### 3.10.3 PHY Control Signals

In addition to the Tx and Rx pairs routed between the FPGA and the PHY, there are also control signals which should be constrained properly in the user's target FPGA design.

| Signal | Type | Description | FPGA Pin | Default Condition |
|---|---|---|---|---|
| MDC | Input to PHY | Management Data Clock Reference for serial management interface | AY13 | |
| MDIO | Input to PHY | Management data: transfers management data in and out of PHY registers synchronously to MDC | AY14 | Pulled High |
| RESET_L | Input to PHY | Active low hardware reset. Pulled high for normal operation. To activate, must be pulled low for a minimum of 400ns. (10 periods of 25MHz reference clock). | AT15 | Pulled High (Normal operation) |
| COMA | Input to PHY | Active high PHY circuitry disable. In COMA mode, PHY draws minimum power. Target FGPA design must pull low to operate Ethernet link. | AU16 | Pulled High (PHY disabled) |
| INT_L | Output from PHY | Active low interrupt | F12 | Pulled High |

**Table 14: PHY Control Signals**

### 3.10.4 Default PHY Configuration

Strapping pins on the Marvell 88E1111 PHY are used to define its configuration on power-up. The following defaults apply:

| Configuration Option | Default |
|---|---|
| PHY Address | 00010 |
| Enable Pause | False |
| Auto-Negotiation Configuration | Auto-Negotiate, Advertise All Capabilities, Prefer Slave |
| Enable Cross-Over | True |
| Enable 125MHz Output Clock | False |
| Hardware Configuration Mode | SGMII without clock with SGMII Auto-Neg to Copper |
| Enable fiber/copper auto selection | False* |
| Enable Energy Detect | True |
| Interface Select | MDC/MDIO |
| Interrupt Polarity | Active Low |
| 75/50 Ohm Termination for Fiber/SGMII | 50 Ohm |

**Table 15: Default PHY Configuration**

*In PCB Revision 1.0, Enable fiber/copper auto selection is True by default.

## 3.11 Memory Interfaces

The **ADM-XRC-6TGE** has four independent banks of DDR3 SDRAM. Each bank consists of two 16 bit wide memory devices in parallel to provide a 32 bit datapath capable of running up to 400MHz (DDR-800). 1Gb devices (Micron MT41J64M16-187E) are fitted as standard to provide 256MB per bank. 2Gb devices (giving 512MB per bank) are available as an ordering option.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). **Figure 11, "DRAM Banks"** Shows the component references and FPGA banks used. Full details of the interface, signaling standards and an example design are provided in the SDK.

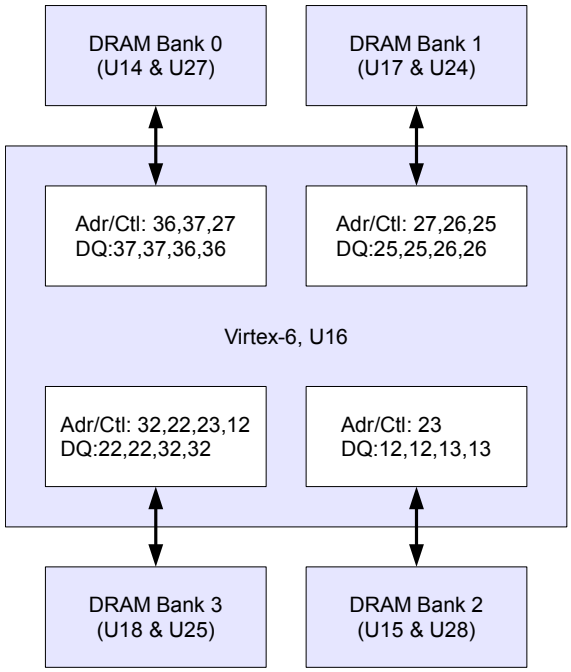



**Figure 11: DRAM Banks**

## 3.12 XRM Interface and Front-Panel I/O

The XRM interface provides a high-performance and flexible front-panel interface through a range of interchangeable XRM modules. Further details of the XRM modules can be found on the Alpha Data website.

The XRM interface consists of two samtec connectors, CN1 and CN2.

### 3.12.1 XRM Connector, CN1

Connector CN1 is for general-purpose signals, power and module control. The connector is a 180-way Samtec connector with 3 fields.

The part fitted to the **ADM-XRC-6TGE** is Samtec QSH-090-01-F-D-A-K.

Full pinout information for this connector is listed in **Appendix B1, "XRM Connector CN1, Field 1"** to **Appendix B3, "XRM Connector CN1, Field 3"**.

### 3.12.2 XRM Connector CN2

Connector CN2 is for the high-speed serial (MGT) links.

The part fitted to the **ADM-XRC-6TGE** is Samtec QSE-014-01-F-D-DP-A-K.

Full pinout information for this connector is listed in **Appendix B4, "XRM Connector CN2"**.

### 3.12.3 XRM I/F - GPIO

The general purpose IO (GPIO) signals are connected in 4 groups to the Target FPGA. Each group consists of 16 standard I/O pairs, a Regional Clock Capable pair and either 2 or 4 single-ended signals. There are no on-board terminations on the pairs and any can be used in single-ended modes.

To allow fast data transfer, all of the GPIO signals within a group are delay matched to within 100ps.

All the XRM GPIO signals and FPGA IO banks share a common voltage, XRM_VIO, that van be either 2.5V, 1.8V or 1.5V. The required voltage is stored within the platform management PROM on the XRM.

| Group | FPGA Bank | Name | Function |
|---|---|---|---|
| Group A | 17 | XRM_DA (15:0) | 16 diff. Pairs / 32 single-ended |
| | | XRM_DA_CC (16) | Regional Clock / GPIO pair / 2 single-ended |
| | | SA (1:0) | 2 single-ended GPIO |
| Group B | 16 | XRM_DB (15:0) | 16 diff. Pairs / 32 single-ended |
| | | XRM_DB_CC (16) | Regional Clock / GPIO pair / 2 single-ended |
| | | SB (1:0) | 2 single-ended GPIO |
| Group C | 15 | XRM_DC (15:0) | 16 diff. Pairs / 32 single-ended |
| | | XRM_DC_CC (16) | Regional Clock / GPIO pair / 2 single-ended |
| | | SC (1:0) | 2 single-ended GPIO |
| Group D | 14 | XRM_DD (15:0) | 16 diff. Pairs / 32 single-ended |
| | | XRM_DD_CC (16) | Regional Clock / GPIO pair / 2 single-ended |
| | | SD (3:0) | 4 single-ended GPIO |

**Table 16: XRM GPIO Groups**

### 3.12.4 XRM I/F - High-speed Serial Links

Eight MGT links are routed between the Target FPGA and the XRM interface. Lanes (6:0) are routed through the Samtec QSE-DP connector, CN2. Lane (7) is routed through the Samtec QSH connector, CN1.

# Appendix A: Rear Connector Pinouts

## A.1: Primary XMC Connector, P5

| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| 1 | PET_PO | PET_NO | 3V3 | PET_P1 | PET_N1 | VPWR |
| 2 | GND | GND | TRST_L | GND | GND | MRSTI_L |
| 3 | PET_P2 | PET_N2 | 3V3 | PET_P3 | PET_N3 | VPWR |
| 4 | GND | GND | TCK | GND | GND | MRSTO_L |
| 5 | PET_P4 | PET_N4 | 3V3 | PET_P5 | PET_N5 | VPWR |
| 6 | GND | GND | TMS | GND | GND | 12V0 |
| 7 | PET_P6 | PET_N6 | 3V3 | PET_P7 | PET_N7 | VPWR |
| 8 | GND | GND | TDI | GND | GND | M12V0 |
| 9 | | | | | | VPWR |
| 10 | GND | GND | TDO | GND | GND | GAO |
| 11 | PER_PO | PER_NO | MBIST_L | PER_P1 | PER_N1 | VPWR |
| 12 | GND | GND | GA1 | GND | GND | MPRESENT_L |
| 13 | PER_P2 | PER_N2 | 3V3_AUX | PER_P3 | PER_N3 | VPWR |
| 14 | GND | GND | GA2 | GND | GND | I2C_SDA |
| 15 | PER_P4 | PER_N4 | | PER_P5 | PER_N5 | VPWR |
| 16 | GND | GND | MVMRO | GND | GND | MSCL |
| 17 | PER_P6 | PER_N6 | | PER_P7 | PER_N7 | |
| 18 | GND | GND | | GND | GND | |
| 19 | REFCLK0_P | REFCLK0_N | | WAKE_L | ROOTO_L | |

**Table A1: Pn5 Interface**

# A.2: Secondary XMC Connector, P6

| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| 1 | PN6_TX_P0 | PN6_TX_N0 | PN6_GPIO_P19 | PN6_TX_P1 | PN6_TX_N1 | PN6_GPIO_N19 |
| 2 | GND | GND | PN6_GPIO_P18 | GND | GND | PN6_GPIO_N18 |
| 3 | PN6_TX_P2 | PN6_TX_N2 | PN6_GPIO_P17 | PN6_TX_P3 | PN6_TX_N3 | PN6_GPIO_N17 |
| 4 | GND | GND | PN6_GPIO_P16 | GND | GND | PN6_GPIO_N16 |
| 5 | PN6_TX_P4 or ETH_DB_N | PN6_TX_N4 or ETH_DB_P | PN6_GPIO_P15 | PN6_TX_P5 or ETH_DA_N | PN6_TX_N5 or ETH_DA_P | PN6_GPIO_N15 |
| 6 | GND | GND | PN6_GPIO_P14 | GND | GND | PN6_GPIO_N14 |
| 7 | PN6_TX_PN6 or ETH_DD_N | PN6_TX_N6 or ETH_DD_P | PN6_GPIO_P13 | PN6_TX_P7 or ETH_DC_N | PN6_TX_N7 or ETH_DC_P | PN6_GPIO_N13 |
| 8 | GND | GND | PN6_GPIO_P12 | GND | GND | PN6_GPIO_N12 |
| 9 | PN6_GPIO_P22 | PN6_GPIO_N22 | PN6_GPIO_P11 | PN6_GPIO_P23 | PN6_GPIO_N23 | PN6_GPIO_N11 |
| 10 | GND | GND | PN6_GPIO_P10 | GND | GND | PN6_GPIO_N10 |
| 11 | Pn6_RX_P0 | Pn6_RX_N0 | PN6_GPIO_P9 | PN6_RX_P 1 | PN6_RX_N 1 | PN6_GPIO_N9 |
| 12 | GND | GND | PN6_GPIO_P8 | GND | GND | PN6_GPIO_N8 |
| 13 | Pn6_RX_P2 | Pn6_RX_N2 | PN6_GPIO_P7 | PN6_RX_P3 | PN6_RX_N3 | PN6_GPIO_N7 |
| 14 | GND | GND | PN6_GPIO_PN6 | GND | GND | PN6_GPIO_N6 |
| 15 | Pn6_RX_P4 | Pn6_RX_N4 | PN6_GPIO_P5 | PN6_RX_P5 | PN6_RX_N5 | PN6_GPIO_N5 |
| 16 | GND | GND | PN6_GPIO_P4 | GND | GND | PN6_GPIO_N4 |
| 17 | Pn6_RX_PN6 | Pn6_RX_N6 | PN6_GPIO_P3 | PN6_RX_P7 | PN6_RX_N7 | PN6_GPIO_N3 |
| 18 | GND | GND | PN6_GPIO_P2 | GND | GND | PN6_GPIO_N2 |
| 19 | REFCLK1_P or PN6_GPIO_P20 | REFCLK1_N or PN6_GPIO_N20 | PN6_GPIO_P1 | PN6_GPIO_P21 | PN6_GPIO_N21 | PN6_GPIO_N1 |

**Table A2: Pn6 Interface**

## A.2.1: Pn6 GPIO Pin Map

| Signal | Clock Capability | FPGA Pin |
|---|---|---|
| PN6_GPIO_P23 | - | AR17 |
| PN6_GPIO_N23 | - | AR18 |
| PN6_GPIO_P22 | - | AN18 |
| PN6_GPIO_N22 | - | AN19 |
| PN6_GPIO_P21 | - | AT16 |
| PN6_GPIO_N21 | - | AU17 |
| PN6_GPIO_P20 | SRCC | AN16 |
| PN6_GPIO_N20 | SRCC | AM16 |
| - | - | - |
| PN6_GPIO_P19 | SRCC | E15 |
| PN6_GPIO_N19 | SRCC | F15 |
| PN6_GPIO_P18 | - | H15 |
| PN6_GPIO_N18 | - | G14 |
| PN6_GPIO_P17 | - | K14 |
| PN6_GPIO_N17 | - | L14 |
| PN6_GPIO_P16 | - | H14 |
| PN6_GPIO_N16 | - | G13 |
| PN6_GPIO_P15 | - | H13 |
| PN6_GPIO_N15 | - | G12 |
| PN6_GPIO_P14 | GC | E14 |
| PN6_GPIO_N14 | GC | F14 |
| PN6_GPIO_P13 | - | D13 |
| PN6_GPIO_N13 | - | E13 |
| PN6_GPIO_P12 | SRCC | J12 |
| PN6_GPIO_N12 | SRCC | J11 |
| PN6_GPIO_P11 | MRCC | M14 |
| PN6_GPIO_N11 | MRCC | N14 |
| PN6_GPIO_P10 | MRCC | M13 |
| PN6_GPIO_N10 | MRCC | N13 |
| PN6_GPIO_P9 | - | C13 |
| PN6_GPIO_N9 | - | D12 |
| PN6_GPIO_P8 | - | B14 |
| PN6_GPIO_N8 | - | C14 |
| PN6_GPIO_P7 | - | A15 |
| PN6_GPIO_N7 | - | A14 |
| PN6_GPIO_P6 | - | C15 |
| PN6_GPIO_N6 | - | D15 |

**Table A3: Pn6 GPIO Pin Map (continued on next page)**

| Signal | Clock Capability | FPGA Pin |
|---|---|---|
| PN6_GPIO_P5 | - | K12 |
| PN6_GPIO_N5 | - | L11 |
| PN6_GPIO_P4 | - | J13 |
| PN6_GPIO_N4 | - | K13 |
| PN6_GPIO_P3 | GC | L12 |
| PN6_GPIO_N3 | GC | M12 |
| PN6_GPIO_P2 | - | D16 |
| PN6_GPIO_N2 | - | C16 |
| PN6_GPIO_P1 | - | A16 |
| PN6_GPIO_N1 | - | B16 |

**Table A3: Pn6 GPIO Pin Map**

GCC: Global clock capable MRCC: Multi-region clock capable SRCC: Single-region clock capable

# A.3: PMC Connector P4

| Signal | FPGA Pin | Clock Capability | P4 Pin | P4 Pin | Clock Capability | FPGA Pin | Signal |
|---|---|---|---|---|---|---|---|
| PN4_P1 | BB16 | - | 1 | 2 | MRCC | AJ16 | PN4_P2 |
| PN4_N1 | BB17 | - | 3 | 4 | MRCC | AJ15 | PN4_N2 |
| PN4_P3 | AN15 | - | 5 | 6 | SRCC | AV13 | PN4_P4 |
| PN4_N3 | AM14 | - | 7 | 8 | SRCC | AV14 | PN4_N4 |
| PN4_P5 | AN14 | MRCC | 9 | 10 | - | AL15 | PN4_P6 |
| PN4_N5 | AN13 | MRCC | 11 | 12 | - | AL14 | PN4_N6 |
| PN4_P7 | AM13 | MRCC | 13 | 14 | - | AY15 | PN4_P8 |
| PN4_N7 | AM12 | MRCC | 15 | 16 | - | AW15 | PN4_N8 |
| PN4_P9 | AP13 | - | 17 | 18 | - | AP16 | PN4_P10 |
| PN4_N9 | AR13 | - | 19 | 20 | - | AP17 | PN4_N10 |
| PN4_P11 | BB13 | - | 21 | 22 | GCC | AP11 | PN4_P12 |
| PN4_N11 | BB14 | - | 23 | 24 | GCC | AP12 | PN4_N12 |
| PN4_P13 | AR12 | - | 25 | 26 | - | BA15 | PN4_P14 |
| PN4_N13 | AT12 | - | 27 | 28 | - | BA14 | PN4_N14 |
| PN4_P15 | AU12 | - | 29 | 30 | - | AV15 | PN4_P16 |
| PN4_N15 | AU13 | - | 31 | 32 | - | AU14 | PN4_N16 |
| PN4_P17 | AW12 | - | 33 | 34 | - | AK18 | PN4_P18 |
| PN4_N17 | AW13 | - | 35 | 36 | - | AJ18 | PN4_N18 |
| PN4_P19 | AM17 | - | 37 | 38 | - | AJ17 | PN4_P20 |
| PN4_N19 | AM18 | - | 39 | 40 | - | AK17 | PN4_N20 |
| PN4_P21 | AL17 | - | 41 | 42 | MRCC | AK15 | PN4_P22 |
| PN4_N21 | AL16 | - | 43 | 44 | MRCC | AK14 | PN4_N22 |
| PN4_P23 | AV16 | - | 45 | 46 | - | BA16 | PN4_P24 |
| PN4_N23 | AW16 | - | 47 | 48 | - | BA17 | PN4_N24 |
| PN4_P25 | AP18 | SRCC | 49 | 50 | - | AR14 | PN4_P26 |
| PN4_N25 | AR19 | SRCC | 51 | 52 | - | AT14 | PN4_N26 |
| PN4_P27 | AT17 | - | 53 | 54 | - | AU19 | PN4_P28 |
| PN4_N27 | AU18 | - | 55 | 56 | - | AT19 | PN4_N28 |
| PN4_P29 | AV18 | - | 57 | 58 | - | AY18 | PN4_P30 |
| PN4_N29 | AV19 | - | 59 | 60 | - | AW18 | PN4_N30 |
| PN4_P31 | BA19 | - | 61 | 62 | - | BB18 | PN4_P32 |
| PN4_N31 | AY19 | - | 63 | 64 | - | BB19 | PN4_N32 |

**Table A4: Pn4 Interface**

GCC: Global clock capable MRCC: Multi-region clock capable SRCC: Single-region clock capable

# A.4: Rear MGT Connections to the Target FPGA

In normal mode, the target FPGA RearMGT lanes (3:0) are connected to the Bridge FPGA. In Bridge Bypass Mode, they are connected to P5 lanes (3:0).

RearMGT Lanes (7:4) are connected directly to P5 lanes (7:4).

RearMGT Lanes (11:8) are connected directly to P6 lanes (3:0).

In the default build configuration, the RearMGT Lane 12 is connected to the Gigabit Ethernet PHY. When the build configuration bypasses the PHY, it is connected directly to P6 Lane 4.

In the default build configuration, the Rx half of RearMGT Lanes (15:13) are connected directly to the Rx half of P6 lanes (7:5) and the Tx half is unconnected (At P6 the Tx pins are used by the 1000Base-T interface). When the build configuration bypasses the PHY, both the Tx and Rx halves are connected directly to P6 Lanes (7:5)).

The pin mappings are as follows in **Table A5 'Target RearMGT Mapping'**

| Signal | Tgt FPGA \"P\" Pin | Tgt FPGA \"N\" Pin |
|---|---|---|
| RearMGT_TX<0> | U1 | U2 |
| RearMGT_TX<1> | T3 | T4 |
| RearMGT_TX<2> | R1 | R2 |
| RearMGT_TX<3> | P3 | P4 |
| RearMGT_TX<4> | W1 | W2 |
| RearMGT_TX<5> | AA1 | AA2 |
| RearMGT_TX<6> | AC1 | AC2 |
| RearMGT_TX<7> | AE1 | AE2 |
| RearMGT_TX<8> | AG1 | AG2 |
| RearMGT_TX<9> | AH3 | AH4 |
| RearMGT_TX<10> | AJ1 | AJ2 |
| RearMGT_TX<11> | AK3 | AK4 |
| RearMGT_TX<12> | AL1 | AL2 |
| RearMGT_TX<13> | AM3 | AM4 |
| RearMGT_TX<14> | AN1 | AN2 |
| RearMGT_TX<15> | AP3 | AP4 |
| | | |
| RearMGT_RX<0> | W5 | W6 |
| RearMGT_RX<1> | V3 | V4 |
| RearMGT_RX<2> | U5 | U6 |
| RearMGT_RX<3> | R5 | R6 |
| RearMGT_RX<4> | Y3 | Y4 |
| RearMGT_RX<5> | AA5 | AA6 |
| RearMGT_RX<6> | AB3 | AB4 |
| RearMGT_RX<7> | AC5 | AC6 |
| RearMGT_RX<8> | AD3 | AD4 |
| RearMGT_RX<9> | AE5 | AE6 |
| RearMGT_RX<10> | AF3 | AF4 |

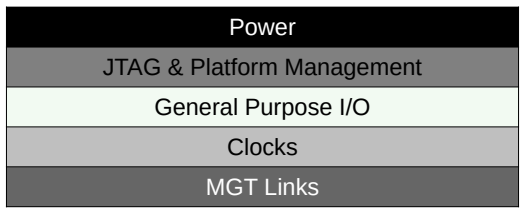
**Table A5: Target RearMGT Mapping (continued on next page)**

| Signal | Tgt FPGA \"P\" Pin | Tgt FPGA \"N\" Pin |
|---|---|---|
| RearMGT_RX<11> | AG5 | AG6 |
| RearMGT_RX<12> | AJ5 | AJ6 |
| RearMGT_RX<13> | AL5 | AL6 |
| RearMGT_RX<14> | AM7 | AM8 |
| RearMGT_RX<15> | AN5 | AN6 |

**Table A5: Target RearMGT Mapping**

# Appendix B: Front (XRM) Connector Pinouts

The XRM interface consists of two connectors: CN1 and CN2. CN1 is a 180-way Samtec QSH in 3 fields. It is for general-purpose signals, power and module control. CN2 is a 28-way Samtec QSE-DP for high-speed serial (MGT) links.



# B.1: XRM Connector CN1, Field 1

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| DA_N0 | N39 | 1 | 2 | M39 | DA_N1 |
| DA_P0 | N38 | 3 | 4 | M38 | DA_P1 |
| DA_N2 | T36 | 5 | 6 | P40 | DA_P3 |
| DA_P2 | U36 | 7 | 8 | P41 | DA_N3 |
| DA_N4 | L40 | 9 | 10 | L42 | DA_N5 |
| DA_P4 | L39 | 11 | 12 | L41 | DA_P5 |
| DA_N6 | T35 | 13 | 14 | R42 | DA_N7 |
| DA_P6 | T34 | 15 | 16 | P42 | DA_P7 |
| DA_P8 | R39 | 17 | 18 | M41 | DA_P9 |
| DA_N8 | P38 | 19 | 20 | M42 | DA_N9 |
| DA_N10 | P37 | 21 | 22 | T40 | DA_N11 |
| DA_P10 | N36 | 23 | 24 | R40 | DA_P11 |
| DA_N12 | R38 | 25 | 26 | N40 | DA_P13 |
| DA_P12 | T39 | 27 | 28 | N41 | DA_N13 |
| DA_N14 | M37 | 29 | 30 | T41 | DA_P15 |
| DA_P14 | M36 | 31 | 32 | T42 | DA_N15 |
| DB_N0 | Y37 | 33 | 34 | V36 | DB_N1 |
| DB_P0 | W37 | 35 | 36 | W36 | DB_P1 |
| SA_0 | N35 | 37 | 38 | P36 | DA_CC_P16 |
| 3V3 | - | 39 | 40 | P35 | DA_CC_N16 |
| 3V3 | - | 41 | 42 | - | FORCE2V5_L |
| 3V3 | - | 43 | 44 | - | 2V5 |
| 5V0 | - | 45 | 46 | - | VREF |
| 5V0 | - | 47 | 48 | - | VccIO |
| VBATT | - | 49 | 50 | - | VccIO |
| 12V0 | - | 51 | 52 | - | VccIO |
| 12V0 | - | 53 | 54 | - | M12V0 |
| PRESENCE_L | - | 55 | 56 | - | TDI |
| TCK | - | 57 | 58 | - | TRST |
| TMS | - | 59 | 60 | - | TDO |

**Table B1: XRM Connector CN1, Field 1**

# B.2: XRM Connector CN1, Field 2

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| DB_N2 | V39 | 61 | 62 | U34 | DB_N3 |
| DB_P2 | U39 | 63 | 64 | V34 | DB_P3 |
| DB_N4 | U38 | 65 | 66 | V35 | DB_N5 |
| DB_P4 | U37 | 67 | 68 | W35 | DB_P5 |
| DB_N6 | U33 | 69 | 70 | W38 | DB_N7 |
| DB_P6 | U32 | 71 | 72 | V38 | DB_P7 |
| DB_N8 | U41 | 73 | 74 | V40 | DB_P9 |
| DB_P8 | U42 | 75 | 76 | W40 | DB_N9 |
| DB_P10 | V33 | 77 | 78 | W41 | DB_N11 |
| DB_N10 | W33 | 79 | 80 | V41 | DB_P11 |
| DB_N12 | Y39 | 81 | 82 | W42 | DB_P13 |
| DB_P12 | Y40 | 83 | 84 | Y42 | DB_N13 |
| DB_N14 | Y35 | 85 | 86 | AA39 | DB_N15 |
| DB_P14 | AA35 | 87 | 88 | Y38 | DB_P15 |
| DB_CC_P16 | W32 | 89 | 90 | AA34 | SB_1 |
| DB_CC_N16 | Y33 | 91 | 92 | AC38 | SC_0 |
| SA_1 | R35 | 93 | 94 | AD36 | SC_1 |
| SB_0 | AA36 | 95 | 96 | AG38 | SD_0 |
| DC_CC_P16 | AD32 | 97 | 98 | AB38 | DC_N1 |
| DC_CC_N16 | AE32 | 99 | 100 | AB37 | DC_P1 |
| DC_N0 | AB36 | 101 | 102 | AH34 | DD_CC_P16 |
| DC_P0 | AC36 | 103 | 104 | AJ35 | DD_CC_N16 |
| SD_1 | AG36 | 105 | 106 | AH35 | SD_3 |
| SD_2 | AJ36 | 107 | 108 | AF30 | GCLK_M2C_N |
| MGTCLK_M2C_P | G10 | 109 | 110 | AE30 | GCLK_M2C_P |
| MGTCLK_M2C_N | G9 | 111 | 112 | - | SDA |
| XRM_PECL_CLK_N | T32 | 113 | 114 | - | SCL |
| XRM_PECL_CLK_P | R32 | 115 | 116 | - | ALERT_N |
| MGT_C2M_P7 | K3 | 117 | 118 | J5 | MGT_M2C_P7 |
| MGT_C2M_N7 | K4 | 119 | 120 | J6 | MGT_M2C_N7 |

**Table B2: XRM Connector CN1, Field 2**

# B.3: XRM Connector CN1, Field 3

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| DC_P2 | AC41 | 121 | 122 | AA42 | DC_P3 |
| DC_N2 | AD41 | 123 | 124 | AB42 | DC_N3 |
| DC_N4 | AC33 | 125 | 126 | AB39 | DC_P5 |
| DC_P4 | AC34 | 127 | 128 | AA40 | DC_N5 |
| DC_P6 | AD42 | 129 | 130 | AC40 | DC_P7 |
| DC_N6 | AE42 | 131 | 132 | AD40 | DC_N7 |
| DC_N8 | AD33 | 133 | 134 | AB41 | DC_N9 |
| DC_P8 | AE33 | 135 | 136 | AA41 | DC_P9 |
| DC_P10 | AF42 | 137 | 138 | AD38 | DC_N11 |
| DC_N10 | AF41 | 139 | 140 | AE38 | DC_P11 |
| DC_P12 | AB32 | 141 | 142 | AD37 | DC_N13 |
| DC_N12 | AB33 | 143 | 144 | AE37 | DC_P13 |
| DC_N14 | AE39 | 145 | 146 | AL42 | DD_P1 |
| DC_P14 | AE40 | 147 | 148 | AM42 | DD_N1 |
| DD_P0 | AK38 | 149 | 150 | AE35 | DC_N15 |
| DD_N0 | AJ38 | 151 | 152 | AE34 | DC_P15 |
| DD_P2 | AJ42 | 153 | 154 | AM41 | DD_N3 |
| DD_N2 | AK42 | 155 | 156 | AL41 | DD_P3 |
| DD_N4 | AG37 | 157 | 158 | AG41 | DD_N5 |
| DD_P4 | AF37 | 159 | 160 | AF40 | DD_P5 |
| DD_P6 | AK40 | 161 | 162 | AL39 | DD_N7 |
| DD_N6 | AL40 | 163 | 164 | AK39 | DD_P7 |
| DD_N8 | AF36 | 165 | 166 | AH41 | DD_N9 |
| DD_P8 | AF35 | 167 | 168 | AG42 | DD_P9 |
| DD_N10 | AJ40 | 169 | 170 | AJ41 | DD_N11 |
| DD_P10 | AH39 | 171 | 172 | AH40 | DD_P11 |
| DD_N12 | AF34 | 173 | 174 | AG39 | DD_N13 |
| DD_P12 | AG34 | 175 | 176 | AF39 | DD_P13 |
| DD_N14 | AG33 | 177 | 178 | AK37 | DD_N15 |
| DD_P14 | AF32 | 179 | 180 | AJ37 | DD_P15 |

**Table B3: XRM Connector CN1, Field 3**

# B.4: XRM Connector CN2

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| MGT_C2M_P0 | J1 | 1 | 2 | H7 | MGT_M2C_P0 |
| MGT_C2M_N0 | J2 | 3 | 4 | H8 | MGT_M2C_N0 |
| | | | | | |
| MGT_C2M_P1 | H3 | 5 | 6 | G5 | MGT_M2C_P1 |
| MGT_C2M_N1 | H4 | 7 | 8 | G6 | MGT_M2C_N1 |
| | | | | | |
| MGT_C2M_P4 | N1 | 9 | 10 | P7 | MGT_M2C_P4 |
| MGT_C2M_N4 | N2 | 11 | 12 | P8 | MGT_M2C_N4 |
| | | | | | |
| MGT_C2M_P5 | M3 | 13 | 14 | N5 | MGT_M2C_P5 |
| MGT_C2M_N5 | M4 | 15 | 16 | N6 | MGT_M2C_N5 |
| | | | | | |
| MGT_C2M_P2 | G1 | 17 | 18 | F7 | MGT_M2C_P2 |
| MGT_C2M_N2 | G2 | 19 | 20 | F8 | MGT_M2C_N2 |
| | | | | | |
| MGT_C2M_P3 | F3 | 21 | 22 | E5 | MGT_M2C_P3 |
| MGT_C2M_N3 | F4 | 23 | 24 | E6 | MGT_M2C_N3 |
| | | | | | |
| MGT_C2M_P6 | L1 | 25 | 26 | L5 | MGT_M2C_P6 |
| MGT_C2M_N6 | L2 | 27 | 28 | L6 | MGT_M2C_N6 |

**Table B4: XRM Connector CN2**

# Appendix C: XRM-IO146 Pinout

The following tables detail the pin-out of the Mictor connector on the XRM-IO146 when fitted to an **ADM-XRC-6TL**.

| Signal | FPGA | Samtec | Mictor | Mictor | Samtec | FPGA | Signal |
|---|---|---|---|---|---|---|---|
| DA_P0 | N38 | 3 | 1 | 2 | 6 | P40 | DA_P3 |
| DA_N0 | N39 | 1 | 3 | 4 | 8 | P41 | DA_N3 |
| DA_P2 | U36 | 7 | 5 | 6 | 4 | M38 | DA_P1 |
| DA_N2 | T36 | 5 | 7 | 8 | 2 | M39 | DA_N1 |
| DA_P4 | L39 | 11 | 9 | 10 | 12 | L41 | DA_P5 |
| DA_N4 | L40 | 9 | 11 | 12 | 10 | L42 | DA_N5 |
| DA_P6 | T34 | 15 | 13 | 14 | 16 | P42 | DA_P7 |
| DA_N6 | T35 | 13 | 15 | 16 | 14 | R42 | DA_N7 |
| DA_P8 | R39 | 17 | 17 | 18 | 18 | M41 | DA_P9 |
| DA_N8 | P38 | 19 | 19 | 20 | 20 | M42 | DA_N9 |
| DA_P10 | N36 | 23 | 21 | 22 | 24 | R40 | DA_P11 |
| DA_N10 | P37 | 21 | 23 | 24 | 22 | T40 | DA_N11 |
| DA_P12 | T39 | 27 | 25 | 26 | 26 | N40 | DA_P13 |
| DA_N12 | R38 | 25 | 27 | 28 | 28 | N41 | DA_N13 |
| DA_P14 | M36 | 31 | 29 | 30 | 30 | T41 | DA_P15 |
| DA_N14 | M37 | 29 | 31 | 32 | 32 | T42 | DA_N15 |
| SA_0 | N35 | 37 | 33 | 34 | 38 | P36 | DA_CC_P16 |
| SA_1 | R35 | 93 | 35 | 36 | 40 | P35 | DA_CC_N16 |
| +5V | - | - | 37 | 38 | 90 | AA34 | SB_1 |

**Table C1: XRM-IO146 Pinout, pins 1 - 38**

| Signal | FPGA | Samtec | Mictor | Mictor | Samtec | FPGA | Signal |
|---|---|---|---|---|---|---|---|
| DB_P0 | W37 | 35 | 39 | 40 | 36 | W36 | DB_P1 |
| DB_N0 | Y37 | 33 | 41 | 42 | 34 | V36 | DB_N1 |
| DB_P2 | U39 | 63 | 43 | 44 | 64 | V34 | DB_P3 |
| DB_N2 | V39 | 61 | 45 | 46 | 62 | U34 | DB_N3 |
| DB_P4 | U37 | 67 | 47 | 48 | 68 | W35 | DB_P5 |
| DB_N4 | U38 | 65 | 49 | 50 | 66 | V35 | DB_N5 |
| DB_P6 | U32 | 71 | 51 | 52 | 72 | V38 | DB_P7 |
| DB_N6 | U33 | 69 | 53 | 54 | 70 | W38 | DB_N7 |
| DB_P8 | U42 | 75 | 55 | 56 | 74 | V40 | DB_P9 |
| DB_N8 | U41 | 73 | 57 | 58 | 76 | W40 | DB_N9 |
| DB_P10 | V33 | 77 | 59 | 60 | 80 | V41 | DB_P11 |
| DB_N10 | W33 | 79 | 61 | 62 | 78 | W41 | DB_N11 |
| DB_P12 | Y40 | 83 | 63 | 64 | 82 | W42 | DB_P13 |
| DB_N12 | Y39 | 81 | 65 | 66 | 84 | Y42 | DB_N13 |
| DB_P14 | AA35 | 87 | 67 | 68 | 88 | Y38 | DB_P15 |
| DB_N14 | Y35 | 85 | 69 | 70 | 86 | AA39 | DB_N15 |
| SD_1 | AG36 | 105 | 71 | 72 | 89 | W32 | DB_CC_P16 |
| SD_2 | AJ36 | 107 | 73 | 74 | 91 | Y33 | DB_CC_N16 |
| +5V | - | - | 75 | 76 | 95 | AA36 | SB_0 |

**Table C2: XRM-IO146 Pinout, pins 39 - 76**

| Signal | FPGA | Samtec | Mictor | Mictor | Samtec | FPGA | Signal |
|---|---|---|---|---|---|---|---|
| DC_P0 | AC36 | 103 | 77 | 78 | 100 | AB37 | DC_P1 |
| DC_N0 | AB36 | 101 | 79 | 80 | 98 | AB38 | DC_N1 |
| DC_P2 | AC41 | 121 | 81 | 82 | 122 | AA42 | DC_P3 |
| DC_N2 | AD41 | 123 | 83 | 84 | 124 | AB42 | DC_N3 |
| DC_P4 | AC34 | 127 | 85 | 86 | 126 | AB39 | DC_P5 |
| DC_N4 | AC33 | 125 | 87 | 88 | 128 | AA40 | DC_N5 |
| DC_P6 | AD42 | 129 | 89 | 90 | 130 | AC40 | DC_P7 |
| DC_N6 | AE42 | 131 | 91 | 92 | 132 | AD40 | DC_N7 |
| DC_P8 | AE33 | 135 | 93 | 94 | 136 | AA41 | DC_P9 |
| DC_N8 | AD33 | 133 | 95 | 96 | 134 | AB41 | DC_N9 |
| DC_P10 | AF42 | 137 | 97 | 98 | 140 | AE38 | DC_P11 |
| DC_N10 | AF41 | 139 | 99 | 100 | 138 | AD38 | DC_N11 |
| DC_P12 | AB32 | 141 | 101 | 102 | 144 | AE37 | DC_P13 |
| DC_N12 | AB33 | 143 | 103 | 104 | 142 | AD37 | DC_N13 |
| DC_P14 | AE40 | 147 | 105 | 106 | 152 | AE34 | DC_P15 |
| DC_N14 | AE39 | 145 | 107 | 108 | 150 | AE35 | DC_N15 |
| SC_0 | AC38 | 92 | 109 | 110 | 97 | AD32 | DC_CC_P16 |
| SC_1 | AD36 | 94 | 111 | 112 | 99 | AE32 | DC_CC_N16 |
| +5V | - | - | 113 | 114 | - | - | +5V |

**Table C3: XRM-IO146 Pinout, pins 77 - 114**

| Signal | FPGA | Samtec | Mictor | Mictor | Samtec | FPGA | Signal |
|---|---|---|---|---|---|---|---|
| DD_P0 | AK38 | 149 | 115 | 116 | 146 | AL42 | DD_P1 |
| DD_N0 | AJ38 | 151 | 117 | 118 | 148 | AM42 | DD_N1 |
| DD_P2 | AJ42 | 153 | 119 | 120 | 156 | AL41 | DD_P3 |
| DD_N2 | AK42 | 155 | 121 | 122 | 154 | AM41 | DD_N3 |
| DD_P4 | AF37 | 159 | 123 | 124 | 160 | AF40 | DD_P5 |
| DD_N4 | AG37 | 157 | 125 | 126 | 158 | AG41 | DD_N5 |
| DD_P6 | AK40 | 161 | 127 | 128 | 164 | AK39 | DD_P7 |
| DD_N6 | AL40 | 163 | 129 | 130 | 162 | AL39 | DD_N7 |
| DD_P8 | AF35 | 167 | 131 | 132 | 168 | AG42 | DD_P9 |
| DD_N8 | AF36 | 165 | 133 | 134 | 166 | AH41 | DD_N9 |
| DD_P10 | AH39 | 171 | 135 | 136 | 172 | AH40 | DD_P11 |
| DD_N10 | AJ40 | 169 | 137 | 138 | 170 | AJ41 | DD_N11 |
| DD_P12 | AG34 | 175 | 139 | 140 | 176 | AF39 | DD_P13 |
| DD_N12 | AF34 | 173 | 141 | 142 | 174 | AG39 | DD_N13 |
| DD_P14 | AF32 | 179 | 143 | 144 | 180 | AJ37 | DD_P15 |
| DD_N14 | AG33 | 177 | 145 | 146 | 178 | AK37 | DD_N15 |
| SD_0 | AG38 | 96 | 147 | 148 | 102 | AH34 | DD_CC_P16 |
| SD_3 | AH35 | 106 | 149 | 150 | 104 | AJ35 | DD_CC_N16 |
| +5V | - | - | 151 | 152 | - | - | +5V |

**Table C4: XRM-IO146 Pinout, pins 115 - 152**

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**Revision History:**

| Date | Revision | Nature of Change |
|---|---|---|
| 6/07/11 | 1.0 | First Release |
| 10/08/11 | 1.1 | Clock Diagram Amendments: Direction of XRM_PECL_CLK, Position of PCIEREFCLK0_VAR |
| 12/08/11 | 1.2 | Amended error in XRM pin-out at pins SD1 and SD2 |
| 30/09/11 | 1.3 | From PCB revision 1.1 onwards the Phy configuration option "Enable fiber/ copper auto selection" is set to False by default |
| 20/01/12 | 1.4 | Amended error in SW1-8 description. |
| 30/01/14 | 1.5 | Amended error in PN4_N5 FPGA pin connection in **Appendix A3, "PMC Connector P4"**. |



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