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XRM-ADC-D2/125

Two Channel Data Acquisition Module

User Guide

Version 1.2

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications

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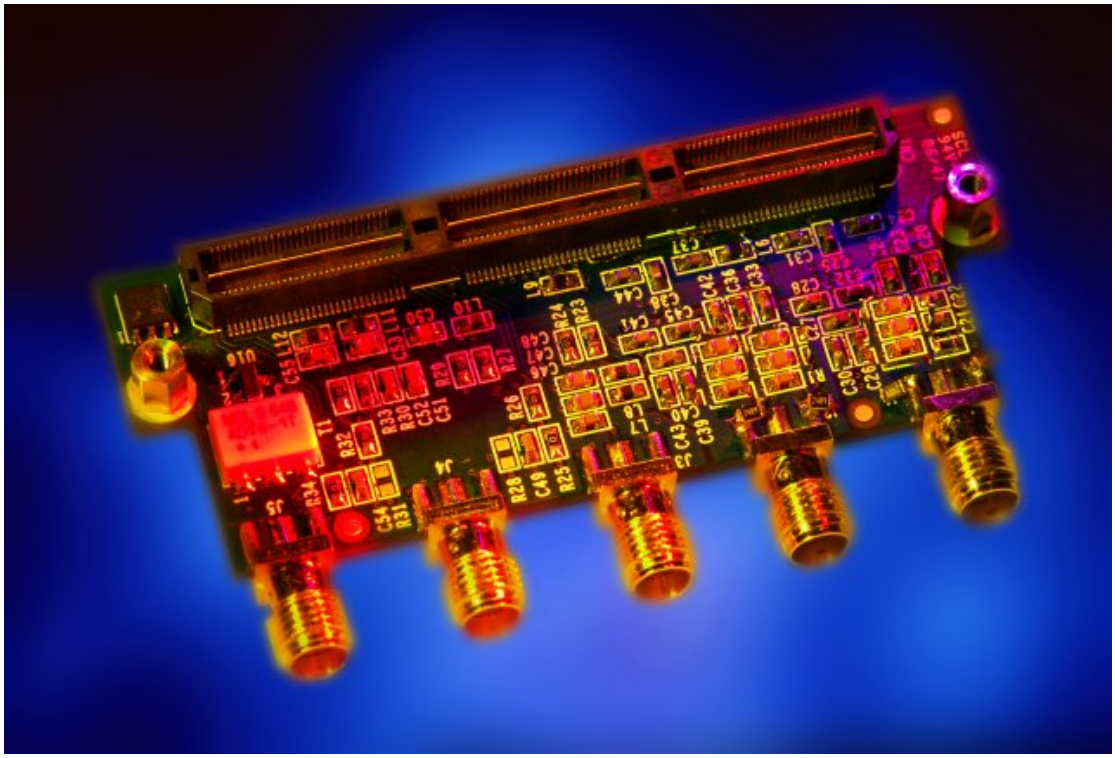


1. Introduction

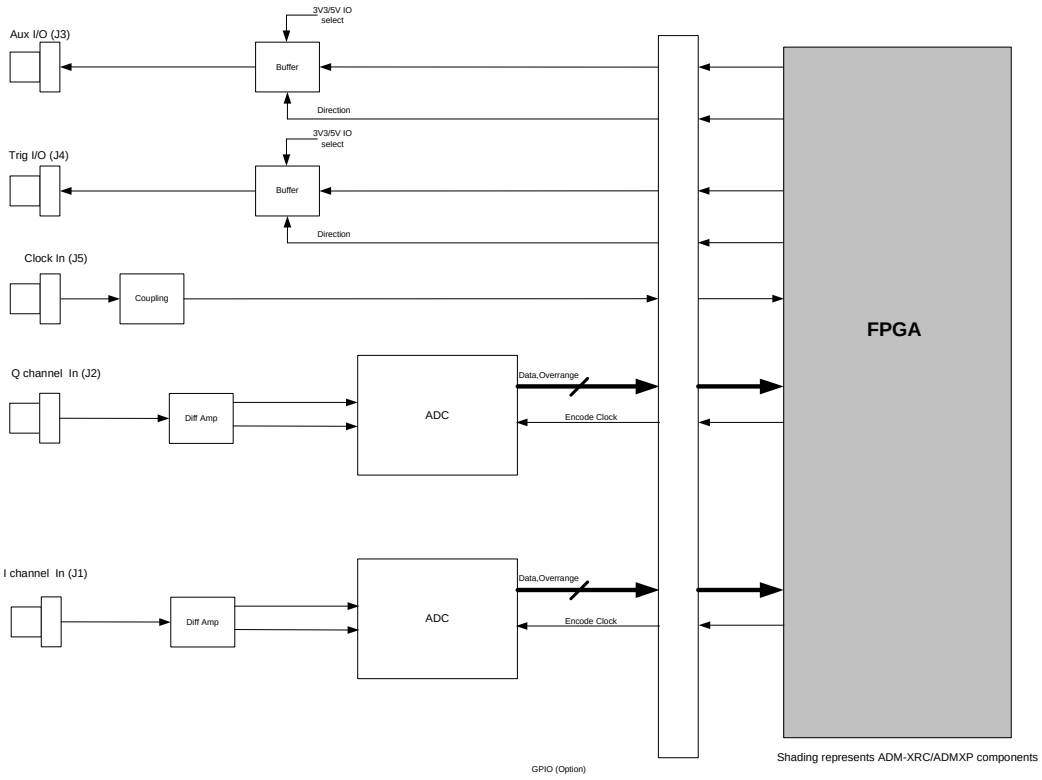
The XRM-ADC-D2/125 is a front panel adapter card designed for use with Alpha Data's ADM-XRCII, ADM-XP, ADM-XRC4 and ADM-XRC5 FPGA-based PMC cards.

The XRM-ADC-D2/125 provides two channels of analogue to digital conversion with 14 bit resolution and supports sampling rates up to 125 MHz It is aimed at applications such as IF/Baseband Signal Sampling.

A number of customisation options are offered with this card, ranging from signal input connector style through to transformer or DC- coupling of inputs.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock

Two auxiliary I/O ports are provided for use as trigger inputs and general purpose signalling.



2. Installation

The XRM-ADC-D2/125 is designed to plug in to the front panel connector (SAMTEC QSH series) on an XRM-ADC II /XPL PMC card. The retaining screws should be tightened to secure the XRM-ADC.

Note: This operation should not be performed while the PMC card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge.
Personnel handling the board should take SSD precautions.
Avoid flexing the board.

3. Specification

3.1. Inputs

3.1.1. I Signal (J1), Q Signal (J2)

Input:	50 Ohms
Bandwidth:	10 Hz to 200 MHz
Level:	+/- 1V =ADC full scale

3.1.2. Clock In (J5)

Input: 50 Ohms, ac coupled
Level: +12 dBm nominal (2.5V pk to pk)

3.2. Input /Output:

3.2.1. Trig IO Port (J4)

User configurable as input or output
Input: 4k7 Ohms, dc coupled
Level: +3V3 LVTTL or +5V TTL (factory/user selectable[1])

3.2.2. Aux. IO Port (J3)

User configurable as input or output
Input: 4k7 Ohms, dc coupled
Level: +3V3 LVTTL or +5V TTL (factory/user selectable[2])

[1] configured via 0R links
[2] configured via 0R links

4. Options

4.1. Connector type

SMA (7 mm, standard)
Long Barrel SMA (20 mm)
SMB
SMC

4.2. Sample Rate

1 MHz to 125 MHz

4.3. Order Code

XRM-ADC-D2/125 –[Connector option] -[IO voltage option]

Fields in square brackets may be omitted in order to obtain the standard configuration for that option. For custom filter designs or other customisation requirements (e.g. connectors) please contact Alpha Data.

5. Related Documents

ADM-XRC-II User Manual
ADM-XP User Manual
ADM-XRC4SX/LX User Manuals
ADM-XRC5 User Manual

6. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

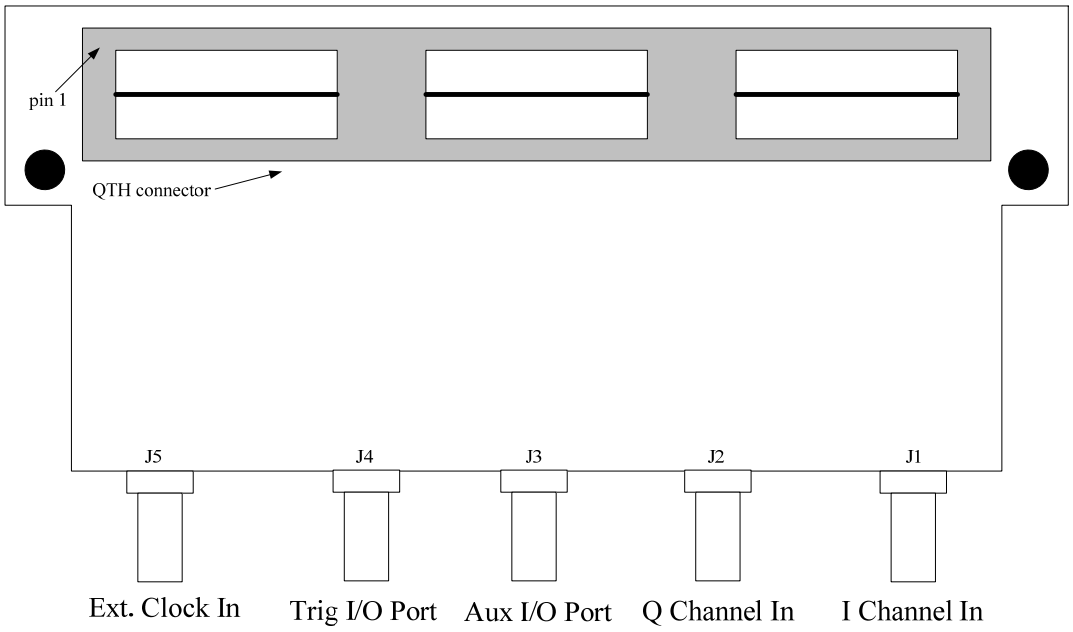
7. Pinout

Samtec Pin No.	UCF Name	XRC2	XPL	XP	XPI	V4SX	V4LX	V5LX	Comments
6	exttrig	C9	D8	H13	H13	N22	N22	AP5	
10	exttrig_dirn	B9	A8	M19	M19	J30	J30	AM7	
14	extaux	D10	D10	L18	L18	R21	R21	AL10	
20	extaux_dirn	G10	B9	F13	F13	K29	K29	AM11	
38	extck_p	H16	C15	F21	F21	D34	D34	AP9	
40	extck_n	H17	B15	G21	G21	E34	E34	AP10	
70	Qchan_d13	G12	C21	C15	C15	AF30	V30	AC9	
72	Qchan_ovr	G13	C20	C14	C14	AF29	W30	AD9	
73	Qchan_oe	E13	G17	H18	H18	AK32	Y33	AH8	
74	Qchan_d12	J14	A21	L16	L16	AA28	T23	AC10	
76	Qchan_d11	J15	B21	M16	M16	AA29	U23	AD10	
78	Qchan_d9	C13	F20	K16	K16	AA30	T25	AG10	
80	Qchan_d10	C14	F19	J16	J16	AB30	T24	AF10	
82	Qchan_d8	H14	E18	H16	H16	AC28	N32	AG11	
84	Qchan_d7	H15	E19	G16	G16	AB28	P32	AF11	
86	Qchan_d6	F16	E20	M17	M17	AD32	T31	AE11	
88	Qchan_d5	F17	D20	M18	M18	AE32	R31	AD11	
90	Qchan_d3	C16	H19	C19	C19	AA24	V34	AH9	
92	Qchan_d4	D17	C23	D19	D19	AA23	V33	W7	
94	Qchan_enc	D18	D23	E28	E28	AD29	U27	AE4	
96	Qchan_d0	C18	E21	F28	F28	AE29	U26	AC3	
98	Qchan_d2	G18	F22	C29	C29	AE31	U31	Y9	
100	Qchan_d1	G19	F21	C28	C28	AF31	U30	W9	
138	Ichan_enc	E21	AC6	C23	C23	AN27	AH34	AE6	
140	Ichan_oe	E22	AC5	D23	D23	AP27	AJ34	AF5	
142	Ichan_d0	B21	J26	G24	G24	AJ29	AA29	AG6	
144	Ichan_d1	B22	J25	H24	H24	AK29	AA28	AF6	
146	Ichan_d2	H22	Y23	K30	K30	AF26	AB30	W1	
148	Ichan_d3	H23	Y24	J30	J30	AE26	AA30	V2	
150	Ichan_d4	D22	H26	K25	K25	AN30	AC30	AH5	
152	Ichan_d5	D23	H25	L25	L25	AP30	AC29	AG5	
154	Ichan_d6	C22	AB25	E24	E24	AE27	Y24	Y1	
156	Ichan_d7	C23	AB26	F24	F24	AF28	W24	W2	
158	Ichan_d8	B23	E28	K23	K23	AL30	AD32	AA3	
160	Ichan_d9	B24	E27	L23	L23	AM30	AE32	AB3	
162	Ichan_d10	F23	AC25	G30	G30	AH27	AE31	AD2	
164	Ichan_d11	F24	AC26	H30	H30	AJ27	AF31	AE2	
166	Ichan_d12	C24	E30	G25	G25	AL29	AF34	AE3	
168	Ichan_d13	D24	E29	H25	H25	AL28	AF33	AF3	
170	Ichan_ovr	G24	AE29	G31	G31	AN24	AB23	AH3	

Analogue data is encoded in 2's complement format, with 0x3FF representing positive full scale and 0x400 representing negative full scale.

OVERRANGE goes high when the signal input is outwith the valid ADC input range.

8. Board Layout



Revision History

Date	Revision	Nature of Change
Nov-2006	1.0	First issue
Jan-2008	1.1	Name Change to XRM-ADC-D2
March 2008	1.2	Minor format changes. Update of copyright