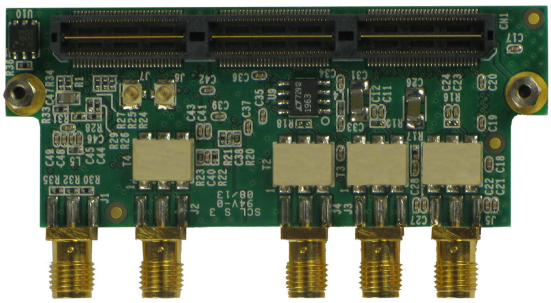


Summary

The **XRM-ADC-D3/1G5** is an I/O Module which provides two Analog to Digital converters with a sampling rate up to 1.5GHz.

The design is based around the ADC08D1500 by National Semiconductors. Both channels are 8-bit resolution and sampling rates up to 1.5GHz. It is aimed at applications such as IF/Baseband Signal Sampling. An external clock source may be used or an internal clock can be used to provide the sampling clock.
An auxiliary I/O port is provided for use as a trigger or general purpose signal.
Separate high speed signals are provided to allow synchronisation across multiple **XRM-ADC-D3/1G5** boards.
The built-in thermal monitor allows the user to check the operating temperature of the ADC. Provided as part of the sample design is the functionality to read the temperature of the device, and software to monitor this and recalibrate the ADC if the thermal drift is sufficient. The software will also shut the ADC down if the device starts to go over the maximum operating temperature.

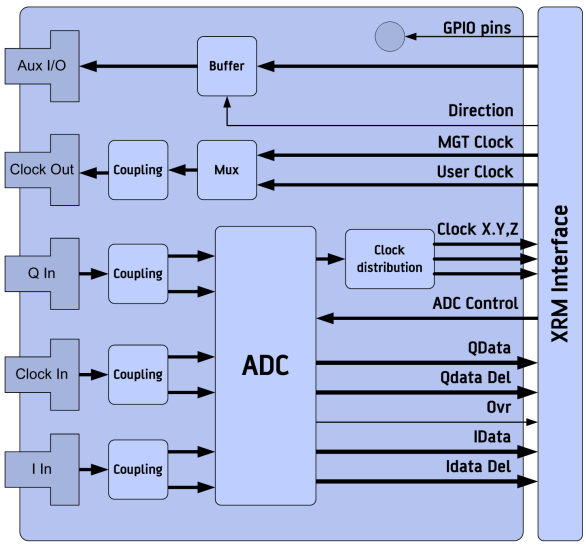
Features

Applications:

- IF/Broadband Signal Sampling

Front Connector I/O:

- Dual 8-bit ADC up to 1.5GHz
- Clock in
- Clock Out
- Auxiliary I/O port
- Dual external synchronisation ports



XRM-ADC-D3/1G5

Specification	
Product Name	XRM-ADC-D3/1G5
Front I/O	**Dual channel ADC:** Dual 8-bit ADC up to 1.5GHz resolution = 8-Bit fmax = 1.5GHz bandwidth = 30MHz to 1700MHz levels = Range1: ±435mV Range2: ±325mV impedance = 50 Ohms connector = SMA SMA-L SMB SMC Range selectable via FPGA and ADC serial port **Note:** Exceeding the maximum voltage limit may result in permanent degradation of converter **Clock in:** Clock in fclock = 200MHz to 1500MHz, single edge sampling 500MHz to 1500MHz, dual edge sampling levels = 424 mV peak to peak (-3.5dBm) nominal, 283 mV peak to peak (-7dBm) minimum up to 1.414 V peak to peak (+7dBm) maximum at SMA connector impedance = 50 Ohms (ac coupled) **Note:** Exceeding the maximum voltage limit may result in permanent degradation of converter **Clock Out:** Clock Out impedance = 50 Ohms, ac coupled levels = ±400mV nominal Source: GTP or User Clock from XRC board. Clock Rate: 20MHz to 500MHz - User clock 300MHz to 1500MHz GTP **Aux IO Port:** Auxiliary I/O port levels = +3V3 LVTTL or +5V TTL (factory/user selectable) impedance = Input: 4k7 Ohms (dc Coupled) **Sync Ports:** Dual external synchronisation ports levels = 2V5 Logic (dc coupled) User configurable as inputs or outputs, signals direct to FPGA pins. **Note:** signals on these connectors must be restricted to 2V5 logic otherwise damage may result.
XRM2	The XRM-ADC-D3/1G5 is also available for XRM2 based FPGA products.
Special Functions	The XRM has built-in thermal monitoring of the ADC
Software	Example UCF, HDL files and Application software are provided with the board.
Environmental	**Temperature:** Air cooled option Operating Temperature 0° to +55°C† † - It is essential that sufficient air-cooling is provided, if thermal monitoring is provided on board then this should be used to shut the device down if it starts to overheat in order to reduce the possibilty of damaging the devices. **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes		
XRM(xver)-ADC-D3/1G5(con)(h)		
XRM Version	xver	blank=Original XRM (FPGA products up to Virtex-5), 2=XRM Version 2 (FPGA products Virtex-6 and later)
Connector Option	con	/blank=SMA(7mm standard), /SMA20=Long Barrel SMA(20mm), /SMB, /SMC
Heatsink	h	blank = No Heastink, /HTSK-XRM-ADC-HS-1 = Heatsink Fitted

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