



ALPHA DATA

XRM-CAMERALINK User Manual

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1 Introduction



Figure 1: XRM-CAMERALINK Module

The XRM-CAMERALINK is a front panel adapter card primarily designed for use with Alpha Data's ADM-XP, ADM-XRCII and ADP-XPI FPGA-based cards. It provides the connectivity between the FPGA card and the industry standard "CameraLink" digital camera interface. It provides the user with the ability to implement computationally-intensive applications such as frame grabbers, digital video communications and image processing systems in FPGA fabric when utilising this type of camera.

The XRM-CAMERALINK board supports the BASE CameraLink configuration and is designed to connect to the remote cameras via the standard 26-way cableform. When used with the example code, any of the formats specified by the BASE configuration may be implemented.

Full user control of the standard camera control lines and serial interface is provided.

LEDs under user control can be programmed to act as link status indicators etc. as required. A site for a 3x2 0.1" pitch header is provided for debugging if required.

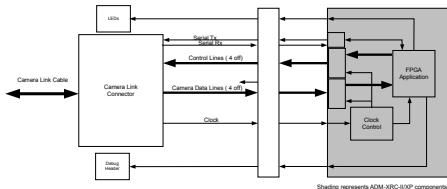


Figure 2: XRM-CAMERALINK Block Diagram

2 Installation

The XRM-CAMERALINK is designed to plug in to the front panel connector (SAMTEC QSH series) on the FPGA base card. The retaining screws should be tightened to secure the XRM-CAMERALINK.

Note: This operation should not be performed while the FPGA card is powered up.

2.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

Avoid flexing the board.

3 Specification

3.1 Connector

26-way Mini D Ribbon (MDR) Connectors manufactured by 3M™ utilising jack-sockets.

3.2 Locking Mechanism

Jack-sockets 3M part number 3341-31

3.3 Cableform

MDR cable assembly, 3M part number 14X26-SZLB-XXX-0LC

XXX= required length in centimetres.

4 Related Documents

ADM-XP User Manual

ADM-XRC-II User Manual

ADP-XPI User Manual

CameraLink Technology Brief (available from Basler Vision Technologies, www.baslerweb.com)

5 Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for users of this card.

6 Pinout

Samtec Pin Number	UCF Name	Direction (FPGA Ssense)	MDR26 Pin	XRC2 FPGA Pin	XP FPGA Pin
1	LED2	Output		C2	D10
2	LED3	Output		E8	C13
3	LED1	Output		B3	E10
4	LED4	Output		E9	D13
89	XCK_P	Gclk Input	9	E16	K21
91	XCK_N	Gclk Input	22	E17	J21
87	XSYNC_P	Input		G17	G19
85	XSYNC_N	Input		G16	H19
64	X0_P	Input	12	C12	J20
62	X0_N	Input	25	C11	H20
67	X1_P	Input	11	B12	L17
65	X1_N	Input	24	B11	K17
72	X2_P	Input	10	G13	C14
70	X2_N	Input	23	G12	C15
75	X3_P	Input	8	E14	G18
73	X3_N	Input	21	E13	H18
100	CC1_P	Input	5	G19	C28
98	CC1_N	Input	18	G18	C29
97	CC2_P	Input	17	J18	G22
99	CC2_N	Input	4	K18	F22
103	CC3_P	Input	3	F19	G27
101	CC3_N	Input	16	F18	H27
102	CC4_P	Input	15	E18	J22
104	CC4_N	Input	2	E19	K22
82	SERTX_P	Output	7	H14	H16
84	SERTX_N	Output	7	H15	G16
83	SER_RX_P	Input	6	K15	J19
81	SER_RX_N	Input	19	K16	K19
107	HEADER<1>	Bidi		A28	K27
106	HEADER<2>	Bidi		F22	L27
96	HEADER<3>	Bidi		C18	F28
92	HEADER<4>	Bidi		D17	D19
90	HEADER<5>	Bidi		C16	C19
94	HEADER<6>	Bidi		D18	E28
7	SPAREP <0>	Bidi		B5	E11
5	SPAREN <0>	Bidi		B4	F11
6	SPAREP <1>	Bidi		C9	H13
8	SPAREN <1>	Bidi		D9	G13

Table 1: XRM_CAMERALINK Pinout (continued on next page)

Samtec Pin Number	UCF Name	Direction (FPGA Ssense)	MDR26 Pin	XRC2 FPGA Pin	XP FPGA Pin
11	SPAREP <2>	Bidi		C6	J10
9	SPAREN <2>	Bidi		D6	H10
12	SPAREP <3>	Bidi		B10	L19
10	SPAREN <3>	Bidi		B9	M19
15	SPAREP <4>	Bidi		J10	F10
13	SPAREN <4>	Bidi		H11	G10
16	SPAREP <5>	Bidi		D11	K18
14	SPAREN <5>	Bidi		KD10	L18
27	SPAREP <6>	Bidi		C8	L13
25	SPAREN <6>	Bidi		C7	M13
26	SPAREP <7>	Bidi		H12	K13
28	SPAREN <7>	Bidi		H13	J13
31	SPAREP <8>	Bidi		A5	K12
29	SPAREN <8>	Bidi		A4	L12
30	SPAREP <9>	Bidi		J11	C11
32	SPAREN <9>	Bidi		J12	C10
35	SPAREP <10>	Bidi		A7	F17
33	SPAREN <10>	Bidi		A6	G17
36	SPAREP <11>	Bidi		K12	G12
34	SPAREN <11>	Bidi		J13	F12

Table 1: XRM_CAMERALINK Pinout

7 Board Layout

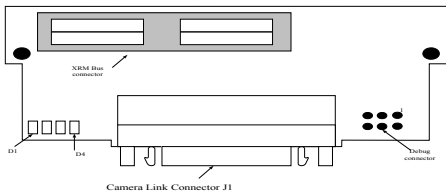


Figure 3: XRM-CAMERALINK Board Layout

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Revision History:

Date	Revision	Nature of Change
November 2004		Initial draft
January 2005	1.0	First release.
September 2005	1.1	Added MDR-26 pinout
23/11/10	1.3	Conversion to XML

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