XRM-CLINK-MINI User Manual

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1 Introduction

The XRM-MINI-CLINK is a front panel adapter card designed for use with Alpha Data's ADM-XRCII, ADM-XP and ADM-XRC4 FPGA-based PMC cards and provides the user with the ability to implement computationally-intensive applications such as frame grabbers, digital video communications and image processing systems in FPGA fabric. The adapter can also be used with the ADP-XPI PCI/PCI-X card to implement applications which in addition require large memory (currently 4 x 4Gbyte DIMMs) for multiple image acquisition, storage and manipulation.

The adapter provides the connectivity between the FPGA card and the industry standard "CameraLink" high-speed digital camera interface using the standard Shrunk Delta Ribbon Connectors from 3M.

The XRM-MINI-CLINK provides support for FULL, MEDIUM and BASE configurations. When used with the example code, any of the formats specified by the BASE configuration may be implemented. Full user control of the standard camera control lines and serial interface is provided.

Factory-configurable options provide support for "Power over Camera Link" (PoCL) with fault protection and current limiting and/or operation as a dual BASE style interface.

Four LEDs are provided for use as status indicators. An RS232 interface and uncommitted FPGA connections are provided for debug purposes.

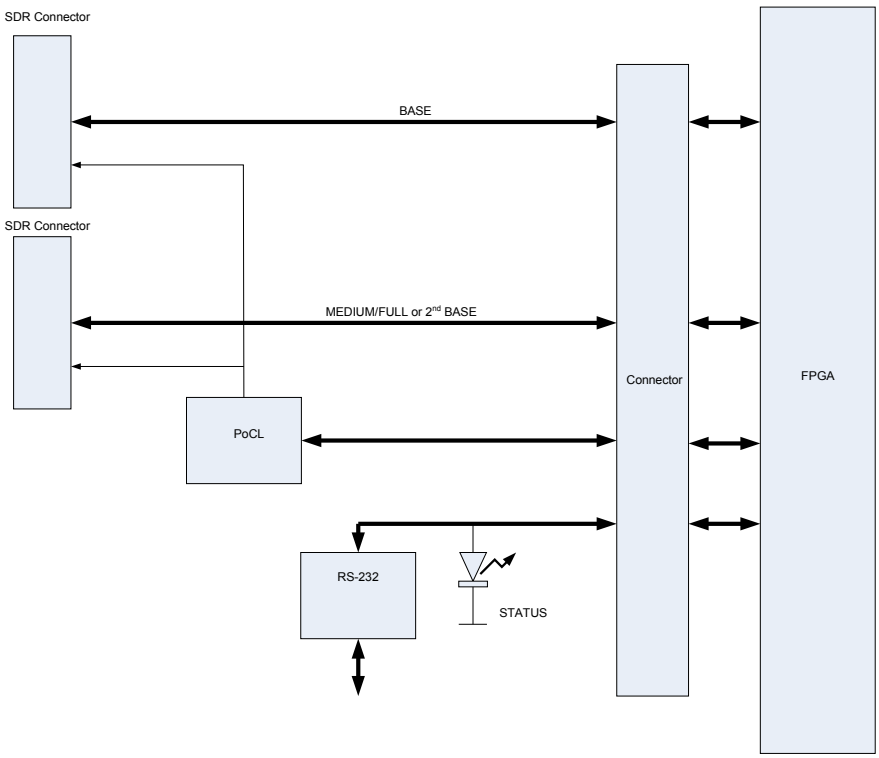

Figure 1: XRM-CLINK-MINI Block Diagram

2 Installation

The XRM-MINI-CLINK is designed to plug in to the front panel connector (SAMTEC QSH series) on an XRM-ADC II / XP/XRC4 PMC card or ADP-XPI PCI/PCI-X card. The retaining screws should be tightened to secure the XRM-ADC.

Note: This operation should not be performed while the host PMC or PCI card is powered up.

2.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

Avoid flexing the board.

3 Specification

3.1 Connectors

SDR connector 3M™ part number 12226-8250-00FR

3.2 Mating Cableform

SDR cable assembly 3M™ part number 1SF26-L120-00C-XXX,

where XXX= length in centimetres.

SDR to MDR cable assembly 3M™ part number 1MF26-L560-00C-XXX, where XXX= length in centimetres.

3.3 Power Over Camera Link (PoCL)

The 'Power over Camera Link' (PoCL) implementation provides +12V to the camera via the lines normally used for camera control signals CC3 and CC4 (frame grabber pins 2,3,15 and16; camera pins 11,12, 24 and 25). This provides +12V @ 350 mA on pins 2 and 3, return on pins 15 and 16 for each connector configured for BASE operation.

This is a factory fit option only.

3.4 Miscellaneous

RS232 transceiver controlled from FPGA implementing 3-wire interface. Connection via 0.1" header.

4 Order Code

XRM-CAMERALINK-FULL-[Interface option] -[PoCL option]

[Interface option] is omitted for FULL/MEDIUM/BASE support for a single camera. Specify 'DUAL' in this field for two independent BASE interfaces capable of supporting two cameras.

[PoCL option] is omitted for normal (no PoCL support) option. Specify 'PoCL' in this field for PoCL implementation.

For further information please contact Alpha Data.

5 Related Documents

ADM-XRC-II User Manual

ADM-XP User Manual

ADM-XRC-4 User Manual

ADP-XPI User Manual

Camera Link Specification v1.1 (Automated Imaging Association)

6 Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for for purchasers of this card.

7 Pinout

7.1 BASE Connector

Frame Grabber Signal Name	XRC2	XP	XPI	XRC4LX(SX)	Samtec pin	SDR pin
X0_p	E9	D13	D13	C32 (C32)	4	12
X0_n	E8	C13	C13	D32 (D32)	2	25
X1_p	B10	L19	L19	J29 (J29)	12	11
X1_n	B9	M19	M19	J30 (J30)	10	24
X2_p	D11	K18	K18	P22 (P22)	16	10
X2_n	D10	L18	L18	R21 (R21)	14	23
X3_p	H9	F9	F9	L30 (L30)	24	8
X3_n	H10	E9	E9	L31 (L31)	22	21
Xck_p	H16	F21	F21	D34 (D34)	38	9
Xck_n	H17	G21	G21	E34 (E34)	40	22
Ser_RX_p	J11	C11	C11	L28 (L28)	30	6
Ser_RX_n	J12	C10	C10	L29 (L29)	32	19
Ser_TX_p	H12	K13	K13	M32 (M32)	26	20
Ser_TX_n	H13	J13	J13	M33 (M33)	28	7
CC1_p	K12	G12	G12	M27 (M27)	36	5
CC1_n	J13	F12	F12	M28 (M28)	34	18
CC2_p	A7	F17	F17	P24 (P24)	35	17
CC2_n	A6	G17	G17	R24 (R24)	33	4
CC3_p/+12V	B12	L17	L17	N27 (N27)	67	3
CC3_n/GND	B11	K17	K17	P27 (P27)	65	16
CC4_p/GND	C12	J20	J20	K32 (K32)	64	15
CC4_n/+12V	C11	H20	H20	K33 (K33)	62	2

Table 1: XRM_CLINK-MINI Base Connector Pinout

Signal names in the VHDL files have the suffix '_a' to distinguish them from the second BASE channel

7.2 FULL/MEDIUM, 2nd BASE Connector

Frame Grabber Signal Name	XRC2	XP	XPI	XRC4LX(SX)	Samtec pin	SDR pin
Y0_p (X0_p)	G13	C14	C14	W30 (AF29)	72	12
Y0_n (X0_n)	G12	C15	C15	V30 (AF30)	70	25
Y1_p (X1_p)	C14	J16	J16	T24 (AB30)	80	11
Y1_n (X1_n)	C13	K16	K16	T25 (AA30)	78	24
Y2_p (X2_p)	F17	M18	M18	R31 (AE32)	88	10
Y2_n (X2_n)	F16	M17	M17	T31 (AD32)	86	23
Y3_p (X3_p)	G19	C28	C28	U30 (AF31)	100	8
Y3_n (X3_n)	G18	C29	C29	U31 (AE31)	98	21
Yck_p (Xck_p)	E16	K21	K21	P34 (AD34)	89	9
Yck_n (Xck_n)	E17	J21	J21	R34 (AC34)	91	22
(SerTX_p)	F19	G27	G27	U32 (AJ34)	103	20
(SerTX_n)	F18	H27	H27	U33 (AH34)	101	7
Z0_p (SerRX_p)	E22	D23	D23	AJ34 (AP27)	140	6
Z0_n (SerRX_n)	E21	C23	C23	AH34 (AN27)	138	19
Z1_p (CC1_p)	B22	H24	H24	AA28 (AK29)	144	5
Z1_n (CC1_n)	B21	G24	G24	AA29 (AJ29)	142	18
Z2_p (CC2_p[1])	D23	L25	L25	AC29 (AP30)	152	4
Z2_n (CC2_n)	D22	K25	K25	AC30 (AN30)	150	17
Z3_p (CC4_p/+12V)	B24	L23	L23	AE32 (AM30)	160	2
Z3_n (CC4_n/GND)	B23	K23	K23	AD32 (AL30)	158	15
Zck_p	E18	J22	J22	AA25 (AN22)	102	3
Zck_n	E19	K22	K22	AA26 (AN23)	104	16
(CC3_p/+12V)	E18	J22	J22	AC28 ()	102	3
(CC3_n./GND)	E19	K22	K22	AB28 (AN23)	104	16

Table 2: XRM_CLINK-MINI Full/Medium 2nd Base Connector Pinout

Signal names in brackets are the equivalent signals when configured as a BASE adaptor. Signal names in the VHDL files have the suffix '_b' to distinguish them from the first BASE channel

(1) - The p,n pins for CC2 and CC4 are swapped with respect to p,n for Z2 and Z3 on the camera link connector. This inversion is handled in the FPGA

7.3 Miscellaneous

Signal Name	XRC2	XP	XPI	XRC4LX(SX)	Samtec pin	Notes
LED0	E14	G18	G18	Y32 (AK31)	75	Drive high to illuminate
LED1	E13	H18	H18	Y33 (AK32)	73	Drive high to illuminate
LED2	K15	J19	J19	P29 (AE33)	83	Drive high to illuminate
LED3	K16	K19	K19	R29 (AE34)	81	Drive high to illuminate
POCL_ON	C7	M13	M13	L34 (L34)	25	Active high PSU enable
POCL FAULT_L	C8	L13	L13	L33 (L33)	27	Active low fault indicator
RS232_TX	B5	E11	E11	J27 (J27)	7	RS232-compatible output
RS232_RX	C6	H10	H10	H29 (H29)	11	RS232-compatible input
RS232_FORCE	J10	F10	F10	E32 (E32)	15	Active high enable for RS232 interface
RS232_READY	C2	D10	D10	H28 (H28)	1	Active high
RS232_INVALID_L	B3	E10	E10	H27 (H27)	3	Active low for framing error
DEBUG(0)	G25	F31	F31	AB22(AP24)	172	General purpose pad for debug use
DEBUG(1)	G24	G31	G31	AB23(AN24)	170	General purpose pad for debug use
DEBUG(2)	K22	C30	C30	W32(AH32)	122	General purpose pad for debug use
DEBUG(3)	K23	D30	D30	V32(AH33)	124	General purpose pad for debug use
DEBUG(4)	K20	H23	H23	AM31(AL23)	180	General purpose pad for debug use
DEBUG(5)	K21	J23	J23	AL31(AM23)	178	General purpose pad for debug use
DEBUG(6)	J21	J26	J26	AA33(AL33)	130	General purpose pad for debug use
DEBUG(7)	J22	H26	H26	AA34(AL34)	132	General purpose pad for debug use

Table 3: XRM_CLINK Miscellaneous Signals Pinout

8 Board Layout

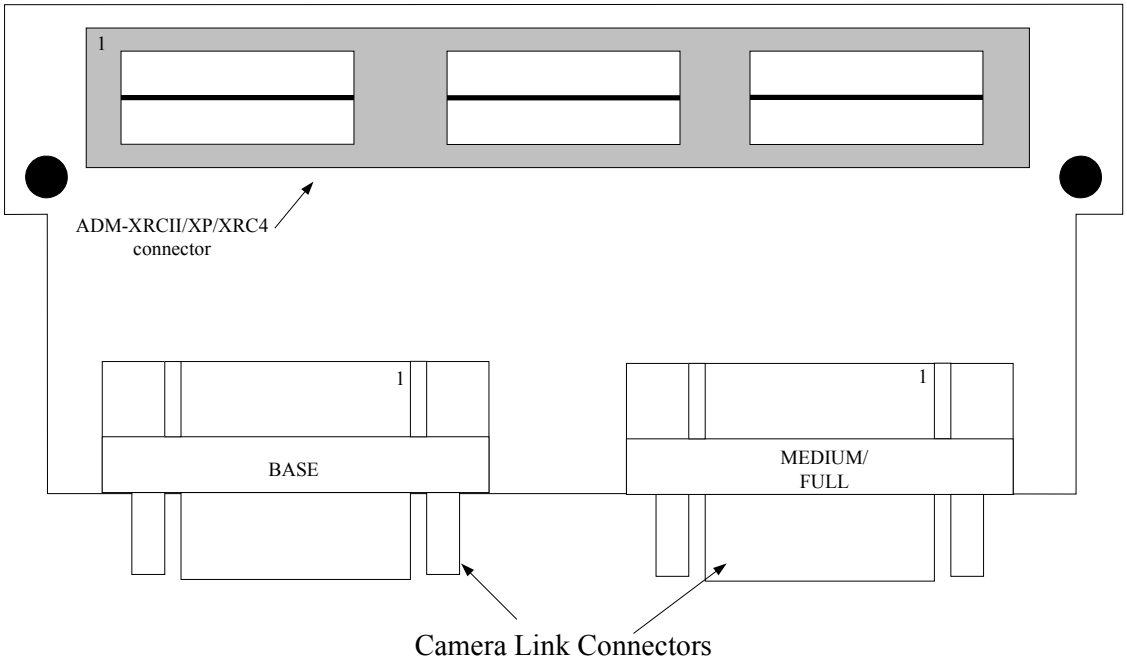

Figure 2: XRM-CLINK-MINI Board Layout (front)

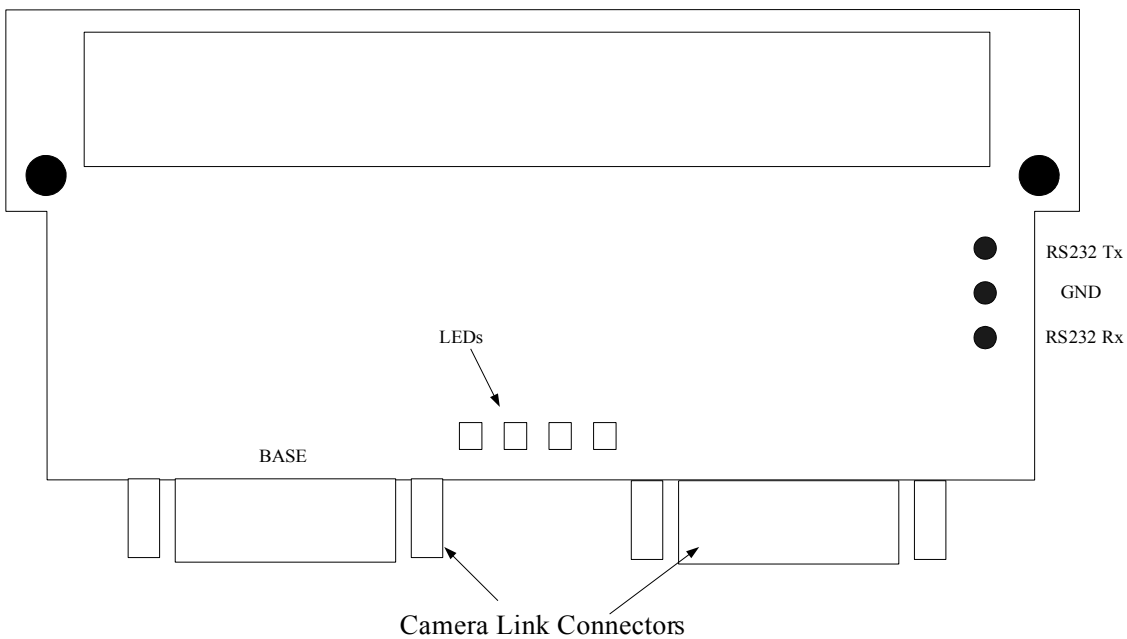

Figure 3: XRM-CLINK-MINI Board Layout (back)

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Revision History:

Date	Revision	Nature of Change
March 2006	1.0	Preliminary issue
July 2006	1.1	Corrected typos, added note.
23/11/10	1.2	Conversion to XML

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