XRM-DDR

DDR Module

User Guide

Version 1.1

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

Table of Contents

1. Introduction

The XRM-DDR is an Alpha Data XRM^{tm} module designed to be used as a front panel adapter for the ADP/ADM range of reconfigurable computing cards. It provides up to 512Mbytes DDR SDRAM memory and 34 user IO lines using a 38 way Mictor connector.

2. Installation

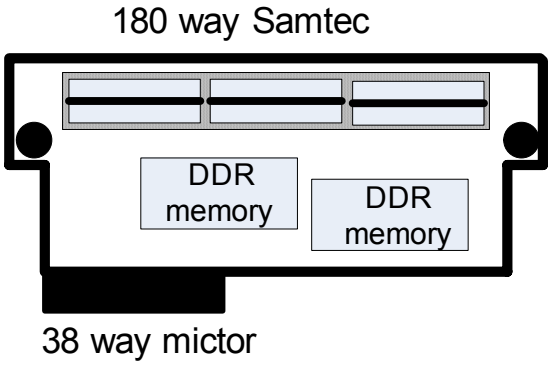
The XRM-DDR is designed to plug in to the front panel connector (SAMTEC QSH series) on ADM-xxx/ADP-xxx cards. The retaining screws should be tightened to secure the XRM-DDR. **The front panel IO voltage on the ADM-xxx/ADP-xxx must be set to 2.5V for this module to function properly**

Note: This operation should not be performed while the PMC/PCI card is powered up.

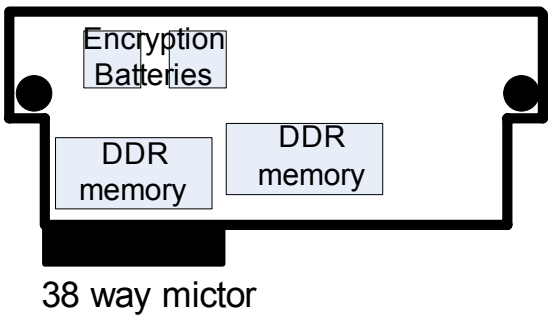
2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

3. Board Layout



Top side – Samtec connector side



Bottom side

4. Specification

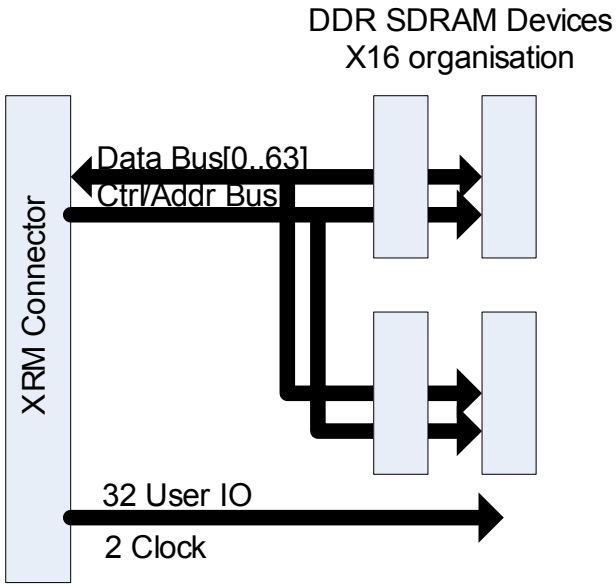
4.1. Memory

Organisation:	Single bank, 64 bit data path
Devices supported:	256Mb, 512Mb or 1Gb DDR SDRAM, TSSOP
Size:	512MByte maximum
Performance:	100MHz (DDR200)

4.2. General Purpose I/O

Number of pairs	16
Number of clocks	1
Max data rate	512Mb/s per pair – dependant on host

4.3. Block diagram



5. General Purpose I/O

The XRM-DDR provides 17 pairs of differential signalling I/O. The Mictor connector is compatible with a wide range of products and is well suited to cabling systems from Precision Interconnect.

The differential pairs on the XRM-DDR are optimised for differential signalling standards that use 100 Ohm impedance. The routing on the board is designed to minimise skew across all the pairs including the designated clock pair.

The user has the choice of using Virtex DCI or DT termination schemes to provide the correct termination for each signal pair used as a receiver.

The XRM-DDR is fitted with resistors to allow the DCI impedance to be selected for ADM-XRC-II/ADM-XP host cards and others that are not fitted with them. The ADM-XRC-4 is fitted with pairs of DCI control resistors for each of the 3 banks that connect to the XRM bus and does require the XRM to provide this function.

Pin	Function	UCF name	Term Res		Pin	Function	UCF name	Term Res	
1	Data[0] +ve	User[0]	R1		2	Data[1] +ve	User[2]	R4	
3	Data[0] -ve	User[1]	-		4	Data[1] -ve	User[3]	-	
5	Data[2] +ve	User[4]	R3		6	Data[3] +ve	User[6]	R2	
7	Data[2] -ve	User[5]	-		8	Data[3] -ve	User[7]	-	
9	Data[4] +ve	User[8]	R5		10	Data[5] +ve	User[10]	R6	
11	Data[4] -ve	User[9]	-		12	Data[5] -ve	User[11]	-	
13	Data[6] +ve	User[12]	R7		14	Data[7] +ve	User[14]	R8	
15	Data[6] -ve	User[13]	-		16	Data[7] -ve	User[15]	-	
17	Data[8] -ve	User[16]	R9		18	Data[9] +ve	User[18]	R10	
19	Data[8] +ve	User[17]	-		20	Data[9] -ve	User[19]	-	
21	Data[10]+ve	User[20]	R11		22	Data[11] +ve	User[22]	R12	
23	Data[10] -ve	User[21]	-		24	Data[11] -ve	User[23]	-	
25	Data[12]+ve	User[24]	R14		26	Data[13] +ve	User[26]	R19	
27	Data[12] -ve	User[25]	-		28	Data[13] -ve	User[27]	-	
29	Data[14]+ve	User[28]	R16		30	Data[15] +ve	User[30]	R17	
31	Data[14] -ve	User[29]	-		32	Data[15] -ve	User[31]	-	
33	nc	nc			34	Clock[0] +ve	User[32]	R64	
35	nc	nc			36	Clock[0] -ve	User[33]	-	
37	+5V fused				38	nc	nc		

6. Memory Interface

6.1. Signalling

All of the DDR memory signals should be driven using SSTL2_I type I/O pins in the FPGA.

6.2. Organisation

Each bank of memory is implemented with two devices each with a separate select signal, active low. Only one select should be active at a time unless the operation used does not cause subsequent contention on the data lines.

6.3. Clocks

Each bank of memory has its own clock and can operate independently of the other.

6.4. Reference Voltage

The XRM-DDR provides VREF back to the host card on Samtec pin 46. This voltage is nominally 1.25V and is dependent on VCCIO, which is normally 2.5V. No other VCCIO voltage is permitted.

6.5. Options for other host cards

The XRM-DDR provides DCI resistors that can be used for control of impedance on ADM-XRC-II cards as shown below.

VRP_0	R14	50R	GND
VRN_0	R13	50R	VCCIO
VRP_1	R1	50R	GND
VRN_1	R2	50R	VCCIO

These resistors do not otherwise affect the operation of the XRM-DDR.

6.6. DRAM Signals

6.6.1. Address Bus

Signal	Samtec Pin No
AD0	62
AD1	64
AD2	66
AD3	68
AD4	70
AD5	72
AD6	74
AD7	76
AD8	78
AD9	80
AD10	82
AD11	85
AD12	84
AD13	155
B0_BA0	86
B0_BA1	88

6.6.2. Control Signals

Signal	Samtec Pin No
CAS	65
CKE	93
RAS	63
WE	67
CS	61

6.6.3. Clocks

Signal	Samtec Pin No
CLK0_N	103
CLK0_P	97
CLK1_N	101
CLK1_P	99
CLK2_N	98
CLK2_P	102
CLK3_N	104
CLK3_P	100

6.6.4. Data Strobes and Masks

Signal	Samtec Pin No
DM0	37
DM1	92
DM2	83
DM3	81
DM4	33
DM5	35
DM6	89
DM7	91
DQS0	71
DQS1	69
DQS2	95
DQS3	87
DQS4	79
DQS5	77
DQS6	75
DQS7	73

6.6.5. Data Bus

Signal	Samtec Pin No
DQ0	107
DQ1	106
DQ2	121
DQ3	123
DQ4	125
DQ5	127
DQ6	129
DQ7	131
DQ8	133
DQ9	135
DQ10	137
DQ11	139
DQ12	141
DQ13	143
DQ14	145
DQ15	147
DQ16	90
DQ17	105
DQ18	122
DQ19	124
DQ20	126
DQ21	128
DQ22	130
DQ23	132
DQ24	134
DQ25	136
DQ26	138
DQ27	140
DQ28	142
DQ29	144
DQ30	146
DQ31	148
DQ32	149
DQ33	151
DQ34	94
DQ35	96
DQ36	157
DQ37	159
DQ38	161
DQ39	163
DQ40	165
DQ41	167
DQ42	169
DQ43	171
DQ44	173
DQ45	175
DQ46	177
DQ47	179
DQ48	150
DQ49	152
DQ50	154
DQ51	156
DQ52	158
DQ53	160
DQ54	162
DQ55	164
DQ56	166
DQ57	168
DQ58	170
DQ59	172
DQ60	174
DQ61	176
DQ62	178
DQ63	180

7. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

Revision History

Date	Revision	Nature of Change
Feb-2005	-	Initial draft