XRM-ETH
User Guide

Document Revision 1.1

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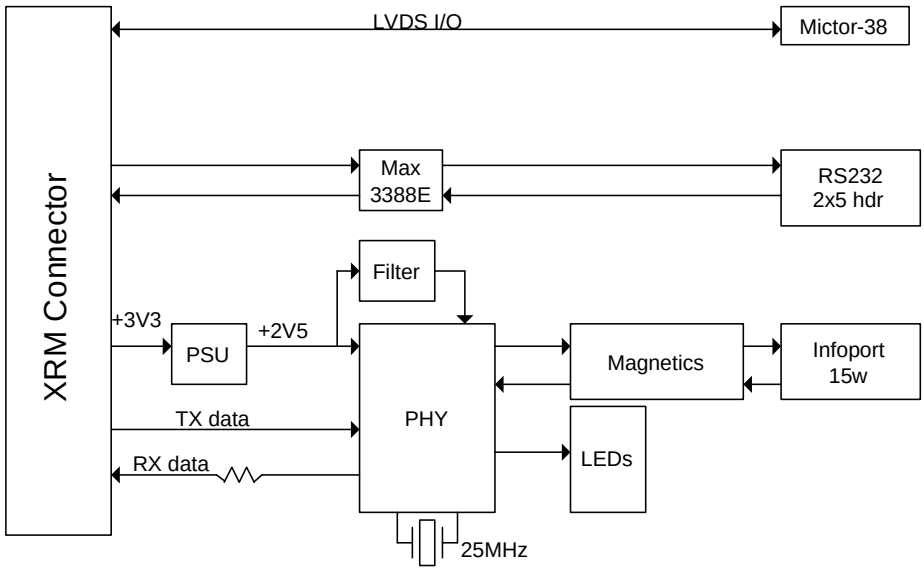
Introduction

The XRM-ETH is a general-purpose adaptor for the ADM-XPL and ADM-XRC-II series of PMC modules. It provides 10/100 Ethernet, RS-232 and general purpose I/O for use with a wide variety of IP.

The XRM-ETH is supplied with two cables to enable connections from the XRM-ETH to 15 way PC COM ports and RJ45 Ethernet.

XRM-ETH-CAB01 for Ethernet
XRM-ETH-CAB02 for RS232

IMPORTANT. The XRM-ETH REV 1 requires the use of 2.5V signalling over the XRM connector and this should be checked prior to power up.



General Purpose I/O

The XRM-ETH provides 18 pairs of differential-capable I/O plus two single-ended signals on a 38 pin Mictor connector. This connector is compatible with a wide range of Mictor connectors and is well suited to cabling systems from Precision Interconnect.

The differential pairs are routed on the XRM-ETH with 100 Ohm impedance and are not terminated to enable direct routing to the FPGA. The user has the choice of using Virtex DCI or DT termination schemes to provide the correct termination for each signal pair. For DCI termination the resistor pairs R1/R2 and R4/R5 should be set to the appropriate value for the desired termination value. By default these resistors are all 100Ohm. The DT scheme can only be used with some Virtex-II PRO devices and provides a fixed 100R termination for LVDS and LDT I/O standards without the power requirement of the DCI option.

RS232 I/O

The XRM-ETH provides two transmit and two receive RS232 signals that can be used for connection to other XPL's or PC COM ports. The supplied cable connects TX0 and RX0 to a standard 15 pin connector suitable for use with a PC. Baud rates up to 115K are supported.

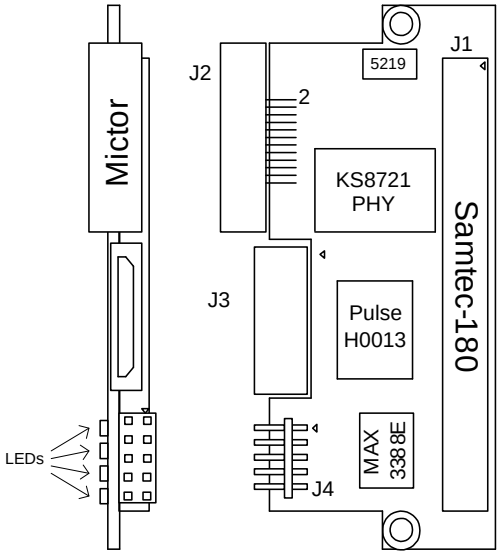
10/100 Ethernet

The XRM-ETH Ethernet capability is supported by a Kendin KS8721B 2.5V PHY. This device is capable of auto-sensing 10 or 100Mb networks and has a standard MII interface suitable for connection to MAC IP in the FPGA. A management interface and reset is also provided.

LEDS are provided on the board and these indicate the following conditions when lit.

D1	Collision
D2	Full Duplex
D3	Speed is 100
D4	Activity

An Ethernet MAC such as the PLB or OPB Ethernet version supplied with EDK6.1i is compatible with this interface.



Input and Output Assignments (ADM-XPL)

Mictor I/O

FPGA		XRM-ETH		
Bank	Pin	Samtec	J2 Mictor	Signal
1	F7	3	1	PAIR_1_P
1	F8	1	3	PAIR_1_N
1	D7	4	2	PAIR_2_P
1	C7	2	4	PAIR_2_N
1	H9	7	5	PAIR_3_P
1	G9	5	7	PAIR_3_N
1	D8	6	6	PAIR_4_P
1	C8	8	8	PAIR_4_N
1	F9	11	9	PAIR_5_P
1	F10	9	11	PAIR_5_N
1	B8	12	10	PAIR_6_P
1	A8	10	12	PAIR_6_N
1	H11	15	13	PAIR_7_P
1	G11	13	15	PAIR_7_N
1	E10	16	14	PAIR_8_P
1	E10	14	16	PAIR_8_N
0	D16	63	17	PAIR_9_P
0	E16	61	19	PAIR_9_N
1	E11	24	18	PAIR_10_P
1	D11	22	20	PAIR_10_N
0	D17	67	21	PAIR_11_P
0	E17	65	23	PAIR_11_N
1	D13	30	22	PAIR_12_P
1	C13	32	24	PAIR_12_N
0	A23	83	25	PAIR_13_P
0	B23	81	27	PAIR_13_N
1	E14	36	26	PAIR_14_P
1	D14	34	28	PAIR_14_N
0	G20	87	29	PAIR_15_P
0	H20	85	31	PAIR_15_N
0	D20	88	30	PAIR_16_P
0	E20	86	32	PAIR_16_N
1	G15	89	33	CLK2
1	F15	91	35	CLK3
1	C15	38	34	CLK0
1	B15	40	36	CLK1
0	H21	95	37	SINGLE_37
0	D21	93	38	SINGLE_38

DCI Terminations

These pins should be prohibited for place and route. These pins have no other purpose on the XRM-ETH.

FPGA		XRM-ETH		
Bank	Pin	Samtec	Value	Signal
1	E24	103	100	VRN_0
1	E25	101	100	VRP_0
1	E6	17	100	VRN_1
1	E7	19	100	VRP_1

Please not that it is not possible to use DCI with Bank 0 when the XRM-ETH is used on the ADM-XP.

Ethernet MAC

All of these signals use VCCFPIO signalling levels. The VCCO selected by the jumper on the XRC-II/XPL should match the IOSTANDARD for these pins.

FPGA		XRM-ETH		
Bank	Pin	Samtec	MAC Signal	Comment
0	C16	62	RXC	O-ST
0	B16	64	TXC	O-ST
0	D18	66	PD	I
0	C18	68	TXER	I
0	H19	90	RXDV	O-PD
0	G22	97	RXD3	O-PD
0	H22	99	RXD2	O-PD
0	C23	92	RXD1	O-PD
0	D23	94	RXD0	O-PD
0	E21	96	TXEN	I
0	F22	98	TXD0	I
0	F21	100	TXD1	I
0	C24	102	TXD2	I
0	D24	104	TXD3	I
0	G23	106	COL	O-PD
0	E23	107	CRS	O-PD
1	C9	18	MDC	I-PU
1	B9	20	MDIO	IO-PU
1	C10	26	RST_N	I-PU
1	C11	28	RXER	O

Key

I	Input
O	Output
O-PD	Output with 2K pulldown
O-ST	Output with 25R source resistor

RS232

FPGA		XRM-ETH		
Bank	Pin	Samtec	J4 Header	Signal
3	AF4	122	1	TX0
3	AF3	124	3	RX0
3	AF2	126	7	TX1
3	AF1	128	9	RX1

The header pin-out is show below.

Signal	Pin	Samtec	Signal
GND	2	1	TX0
GND	4	3	RX0
POL	6	5	NC
GND	8	7	TX1
GND	10	9	RX1

Input and Output Assignments (ADM-XP)

Mictor I/O

FPGA		XRM-ETH		
Bank	Pin	Samtec	J2 Mictor	Signal
1	E10	3	1	PAIR_1_P
1	D10	1	3	PAIR_1_N
1	D13	4	2	PAIR_2_P
1	C13	2	4	PAIR_2_N
1	E11	7	5	PAIR_3_P
1	F11	5	7	PAIR_3_N
1	H13	6	6	PAIR_4_P
1	G13	8	8	PAIR_4_N
1	H10	11	9	PAIR_5_P
1	J10	9	11	PAIR_5_N
1	L19	12	10	PAIR_6_P
1	M19	10	12	PAIR_6_N
1	F10	15	13	PAIR_7_P
1	G10	13	15	PAIR_7_N
1	K18	16	14	PAIR_8_P
1	L18	14	16	PAIR_8_N
1	C20	63	17	PAIR_9_P
1	D20	61	19	PAIR_9_N
1	F9	24	18	PAIR_10_P
1	E9	22	20	PAIR_10_N
1	L17	67	21	PAIR_11_P
1	K17	65	23	PAIR_11_N
1	C11	30	22	PAIR_12_P
1	C10	32	24	PAIR_12_N
1	J19	83	25	PAIR_13_P
1	K19	81	27	PAIR_13_N
1	G12	36	26	PAIR_14_P
1	F12	34	28	PAIR_14_N
1	G19	87	29	PAIR_15_P
1	H19	85	31	PAIR_15_N
1	M18	88	30	PAIR_16_P
1	M17	86	32	PAIR_16_N
1	K21	89	33	CLK2
1	J21	91	35	CLK3
1	F21	38	34	CLK0
1	G21	40	36	CLK1
1	F19	95	37	SINGLE_37
1	E19	93	38	SINGLE_38

DCI Terminations

These pins should be prohibited for place and route. These pins have no other purpose on the XRM-ETH.

FPGA		XRM-ETH		
Bank	Pin	Samtec	Value	Signal
0	G27	103	100	VRN_0
0	H27	101	100	VRP_0
1	G9	17	100	VRN_1
1	H9	19	100	VRP_1

Ethernet MAC

All of these signals use VCCFPIO signalling levels. The VCCO selected by the jumper on the XRC-II/XPL should match the IOSTANDARD for these pins.

FPGA		XRM-ETH		
Bank	Pin	Samtec	MAC Signal	Comment
1	H20	62	RXC	O-ST
1	G20	64	TXC	O-ST
1	F15	66	PD	I
1	E15	68	TXER	I
1	C19	90	RXDV	O-PD
0	G22	97	RXD3	O-PD
0	F22	99	RXD2	O-PD
1	D19	92	RXD1	O-PD
0	E28	94	RXD0	O-PD
0	F28	96	TXEN	I
0	C29	98	TXD0	I
0	C28	100	TXD1	I
0	J22	102	TXD2	I
0	K22	104	TXD3	I
0	L27	106	COL	O-PD
0	K27	107	CRS	O-PD
1	E13	18	MDC	I-PU
1	F13	20	MDIO	IO-PU
1	K13	26	RST_N	I-PU
1	J13	28	RXER	O

Key

I	Input
O	Output
O-PD	Output with 2K pulldown
O-ST	Output with 25R source resistor

RS232

FPGA		XRM-ETH		
Bank	Pin	Samtec	J4 Header	Signal
0	C30	122	1	TX0
0	D30	124	3	RX0
0	M26	126	7	TX1
0	M25	128	9	RX1

The header pin-out is show below.

Signal	Pin	Samtec	Signal
GND	2	1	TX0
GND	4	3	RX0
POL	6	5	NC
GND	8	7	TX1
GND	10	9	RX1

Input and Output Assignments (ADM-XRC-4LX)

Mictor I/O

FPGA		XRM-ETH		
Bank	Pin	Samtec	J2 Mictor	Signal
9	H27	3	1	PAIR_1_P
9	H28	1	3	PAIR_1_N
9	C32	4	2	PAIR_2_P
9	D32	2	4	PAIR_2_N
9	J27	7	5	PAIR_3_P
9	K27	5	7	PAIR_3_N
9	N22	6	6	PAIR_4_P
9	N23	8	8	PAIR_4_N
9	H29	11	9	PAIR_5_P
9	H30	9	11	PAIR_5_N
9	J29	12	10	PAIR_6_P
9	J30	10	12	PAIR_6_N
9	E32	15	13	PAIR_7_P
9	E33	13	15	PAIR_7_N
9	P22	16	14	PAIR_8_P
9	R21	14	16	PAIR_8_N
9	H33	63	17	PAIR_9_P
9	H34	61	19	PAIR_9_N
9	L30	24	18	PAIR_10_P
9	L31	22	20	PAIR_10_N
9	N27	67	21	PAIR_11_P
9	P27	65	23	PAIR_11_N
9	L28	30	22	PAIR_12_P
9	L29	32	24	PAIR_12_N
13	P29	83	25	PAIR_13_P
13	R29	81	27	PAIR_13_N
9	M27	36	26	PAIR_14_P
9	M28	34	28	PAIR_14_N
13	P30	87	29	PAIR_15_P
13	P31	85	31	PAIR_15_N
13	R31	88	30	PAIR_16_P
13	T31	86	32	PAIR_16_N
13	P34/R32	89	33	CLK2
13	R34/R33	91	35	CLK3
9	D34/F33	38	34	CLK0
9	E34/F34	40	36	CLK1
13	T33	95	37	SINGLE_37
13	T34	93	38	SINGLE_38

DCI Terminations

These DCI settings are provided on the ADM-XRC-4 and are by default set to 50R for banks 9 and 13.

Ethernet MAC

All of these signals use VCCFPIO signalling levels. The VCCO selected by the jumper on the XRC-II/XPL should match the IOSTANDARD for these pins.

FPGA		XRM-ETH		
Bank	Pin	Samtec	MAC Signal	Comment
9	K33	62	RXC	O-ST
9	K32	64	TXC	O-ST
9	K34	66	PD	I
9	J34	68	TXER	I
13	V34	90	RXDV	O-PD
11	AG30	97	RXD3	O-PD
11	AG31	99	RXD2	O-PD
13	V33	92	RXD1	O-PD
13	U27	94	RXD0	O-PD
13	U26	96	TXEN	I
13	U31	98	TXD0	I
13	U30	100	TXD1	I
11	AC28	102	TXD2	I
11	AB29	104	TXD3	I
9	H32	106	COL	O-PD
13	V25	107	CRS	O-PD
9	K28	18	MDC	I-PU
9	K29	20	MDIO	IO-PU
9	M32	26	RST_N	I-PU
9	M33	28	RXER	O

Key

I	Input
O	Output
O-PD	Output with 2K pulldown
O-ST	Output with 25R source resistor

RS232

FPGA		XRM-ETH		
Bank	Pin	Samtec	J4 Header	Signal
13	W32	122	1	TX0
13	V32	124	3	RX0
13	Y29	126	7	TX1
13	W29	128	9	RX1

The header pin-out is show below.

Signal	Pin	Samtec	Signal
GND	2	1	TX0
GND	4	3	RX0
POL	6	5	NC
GND	8	7	TX1
GND	10	9	RX1

Example UCF for the ADM-XPL

Copy the following signal constraints into a text file and save as a UCF. Please note that other constraints, especially for timing, may be needed for successful place and route.

```
#
#     Use TX0 and RX0 with the supplied cable.
#
NET  Uart1_sin          LOC = AF3;  # RX0
NET  Uart1_rtsN         LOC = AF2;  # TX1
NET  Uart1_ctsN         LOC = AF1;  # RX1
NET  Uart1_sout         LOC = AF4;  # TX0

#
#     Ethernet MII
#
NET "ETH_TXC"     LOC = "B16"; #
NET "ETH_RXC"     LOC = "C16"; #
NET "ETH_CRS"     LOC = "E23"; #
NET "ETH_CRS"     PULLDOWN;    # RMII_LPBK = DISABLE
NET "ETH_RXDV"    LOC = "H19"; #
NET "ETH_RXDV"    PULLDOWN;    # PCS_LPBK = DISABLE
NET "ETH_RXD<0>"  LOC = "D23"; #
NET "ETH_RXD<1>"  LOC = "C23"; #
NET "ETH_RXD<2>"  LOC = "H22"; #
NET "ETH_RXD<3>"  LOC = "G22"; #
NET "ETH_RXD<0>"  PULLDOWN;    # PHYAD[3:0] = 0000
NET "ETH_RXD<1>"  PULLDOWN;    #
NET "ETH_RXD<2>"  PULLDOWN;    #
NET "ETH_RXD<3>"  PULLDOWN;    #
NET "ETH_COL"     LOC = "G23"; #
NET "ETH_COL"     PULLDOWN;    # RMII = DISABLE
NET "ETH_RXER"    LOC = "C11"; #
NET "ETH_RXER"    PULLDOWN;    # ISOLATE = DISABLE
NET "ETH_TXEN"    LOC = "E21"; #
NET "ETH_TXER"    LOC = "C18"; #
NET "ETH_TXD<0>"  LOC = "F22"; #
NET "ETH_TXD<1>"  LOC = "F21"; #
NET "ETH_TXD<2>"  LOC = "C24"; #
NET "ETH_TXD<3>"  LOC = "D24"; #
NET "ETH_MDC"     LOC = "C9";  #
NET "PHY_RESETn"  LOC = "C10"; #
NET "ETH_MDIO"    LOC = "B9";  #

#
#     Mictor I/O pins in pairs 0/1, 2/3 etc except 36/37 which are
#     single-ended.
#
NET IO<0> LOC= F7 ;
NET IO<1> LOC= F8 ;
NET IO<2> LOC= D7 ;
NET IO<3> LOC= C7 ;
NET IO<4> LOC= H9 ;
NET IO<5> LOC= G9 ;
NET IO<6> LOC= D8 ;
```

```
NET IO<7> LOC= C8 ;
NET IO<8> LOC= F9 ;
NET IO<9> LOC= F10 ;
NET IO<10> LOC= B8 ;
NET IO<11> LOC= A8 ;
NET IO<12> LOC= H11 ;
NET IO<13> LOC= G11 ;
NET IO<14> LOC= E10 ;
NET IO<15> LOC= D10 ;
NET IO<16> LOC= D16 ;
NET IO<17> LOC= E16 ;
NET IO<18> LOC= E11 ;
NET IO<19> LOC= D11 ;
NET IO<20> LOC= D17 ;
NET IO<21> LOC= E17 ;
NET IO<22> LOC= D13 ;
NET IO<23> LOC= C13 ;
NET IO<24> LOC= A23 ;
NET IO<25> LOC= B23 ;
NET IO<26> LOC= E14 ;
NET IO<27> LOC= D14 ;
NET IO<28> LOC= G20 ;
NET IO<29> LOC= H20 ;
NET IO<30> LOC= D20 ;
NET IO<31> LOC= E20 ;
NET IO<32> LOC= G15 ;
NET IO<33> LOC= F15 ;
NET IO<34> LOC= C15 ;
NET IO<35> LOC= B15 ;
NET IO<36> LOC= H21 ;
NET IO<37> LOC= D21 ;
```