XRM-HD-SDI

HD SDI Adaptor Module

User Guide

Version 1.1

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

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Photograph 1 - XRM-HD-SDI

1. Introduction

The XRM-HD-SDI is a front panel adapter card primarily designed for use with Alpha Data's ADM-XRCI4, ADM-XP, ADM-XRCII and ADP-XPI FPGA-based cards.

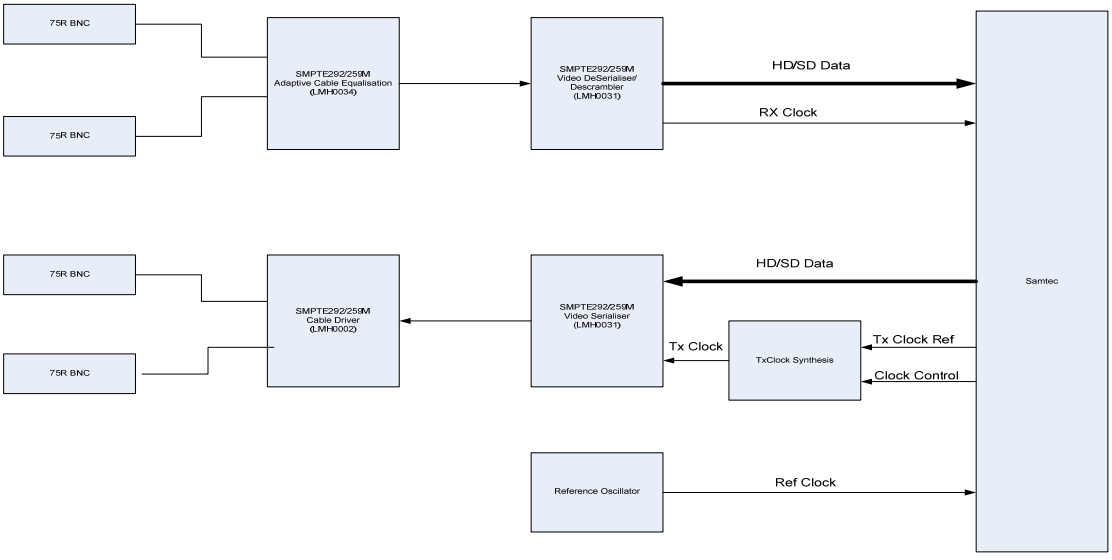
This adapter provides users with an easy method of applying Alpha Data's range of FPGA cards to tasks involving compute-intensive processing of HDTV or SDTV serial data streams.

Connectivity to both input and output streams are provided using industy-standard 75 ohm BNC connectors. Input and output channels can be independently configured as balanced or unbalanced.

Automatic cable equalisation is provided for the input stream whilst the output stream is buffered by a cable driver which can be configured for either SD or HD operation.
Both the cable equaliser and driver are compatible with DVB-ASI, SMPTE 292M, SMPTE 344M and SMPTE 259M specifications.

The serialiser/deserialiser (SERDES) interface provides automatic recognition of numerous standard formats. BIST and video pattern generator on both receive and transmit devices provides users with the ability to diagnose fault locations with the minimum of disruption to hardware connections.

Full user access and control of all SERDES features via interface registers and pins is provided.



2. Installation

The XRM-HD-SDI is designed to plug in to the front panel connector (SAMTEC QSH series) on the FPGA base card. The retaining screws should be tightened to secure the XRM-HD-SDI.

Note: This operation should not be performed while the FPGA card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

2.2. Voltage Settings

This board is a 3V3 only module; users should ensure that the VIO setting on the FPGA card is set to suit this value to ensure no damage can occur.

3. Specification

3.1. Inputs

DIN+ : AC coupled, 75 ohm termination via 75 ohm BNC.

DIN- : AC coupled, 75 ohm termination via 75 ohm BNC.
Input voltage swing: 800 mV peak to peak nominal[1]

3.2. Output

DOUT+: AC coupled, 75 ohm termination via 75 ohm BNC.
DOUT- : AC coupled, 75 ohm termination via 75 ohm BNC.
Output voltage swing : 800 mV peak to peak [2] [3]

3.3. Clocks

An on-board 108 MHz crystal oscillator is used as a low-jitter clock source to provide 27MHz, 36MHz and 54MHz clocks which is used by the receive circuit as a timing reference for clock and data recovery.

The transmit circuit can also access these clocks directly clocks or can use these as a reference clock to drive a low-jitter synthesiser which provides 74.25MHz and 74.175824 MHz for use with HDTV formats in addition to other standard clock frequencies.

[1] When used in single-ended mode, the unconnected port should be loaded with a 75R termination for optimum performance.
[2] When used in single-ended mode, the unconnected port should be loaded with a 75R termination for optimum performance.
[3] single-ended into 75 ohm load

4. Related Documents

ADM-XRC5 User Manual
ADM-XRC4 User Manual
ADM-XP User Manual
ADM-XRC-II User Manual
ADP-XPI User Manual

5. Design Examples

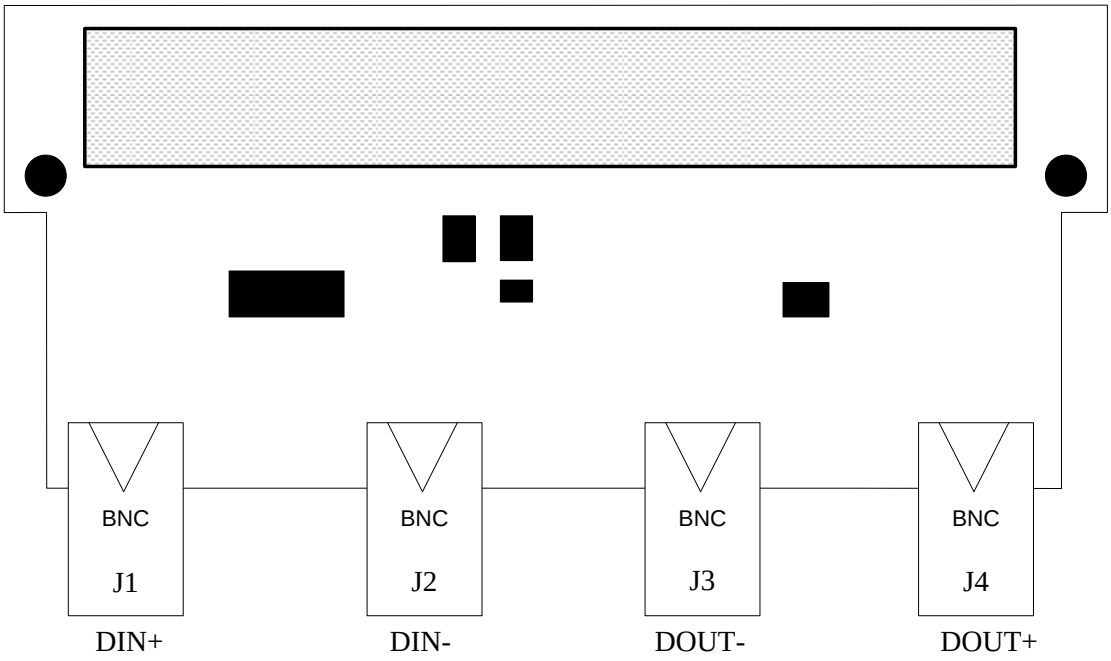
Example UCF, HDL files and Application software are available from Alpha Data for users of this card.

6. Pinout

Samtec Pin No.	UCF Name	XRC2	XP	XPI	V4SX	V4LX	V5LX	Comments
1	eq_cdbar_mute	C2	D10	D10	H28	H28	AL6	
3	eq_bypass	B3	E10	E10	H27	H27	AL5	
5	rx_aux(9)	B4	F11	F11	K27	K27	AL4	
6	rx_rd_wrbar	C9	H13	H13	N22	N22	AP5	
7	rx_aux(8)	B5	E11	E11	J27	J27	AM5	
8	rx_anc_ctrlbar	D9	G13	G13	N23	N23	AP4	
9	rx_aux(7)	D6	J10	J10	H30	H30	AM6	
10	rx_aux(5)	B9	M19	M19	J30	J30	AM7	
11	rx_aux(6)	C6	H10	H10	H29	H29	AN7	
12	rx_aux(4)	B10	L19	L19	J29	J29	AM8	
13	rx_aux(3)	H11	G10	G10	E33	E33	AN8	
14	rx_aux(1)	D10	L18	L18	R21	R21	AL10	
15	rx_aux(2)	J10	F10	F10	E32	E32	AN9	
16	rx_aux(0)	D11	K18	K18	P22	P22	AM10	
17	rx_aclk	F8	G9	G9	C33	C33	AP7	
18	rx_iopins(6)	G11	E13	E13	K28	K28	AN10	
19	rx_iopins(7)	F9	H9	H9	C34	C34	AP6	
20	rx_iopins(5)	G10	F13	F13	K29	K29	AM11	
21	rx_iopins(4)	B6	J12	J12	G33	G33	AM17	
22	rx_iopins(2)	H10	E9	E9	L31	L31	AP17	
23	rx_iopins(3)	B7	H12	H12	G32	G32	AN17	
24	rx_iopins(1)	H9	F9	F9	L30	L30	AP16	
25	rx_hdluma(9)	C7	M13	M13	L34	L34	AP12	
26	rx_iopins(0)	H12	K13	K13	M32	M32	AM15	
27	rx_hdluma(8)	C8	L13	L13	L33	L33	AP11	
29	rx_hdluma(5)	A4	L12	L12	R19	R19	AN14	
30	rx_hdluma(7)	J11	C11	C11	L28	L28	AP15	
31	rx_hdluma(4)	A5	K12	K12	P20	P20	AP14	
32	rx_hdluma(6)	J12	C10	C10	L29	L29	AN15	
33	rx_hdluma(1)	A6	G17	G17	R24	R24	AA11	
34	rx_hdluma(3)	J13	F12	F12	M28	M28	AA9	
35	rx_hdluma(0)	A7	F17	F17	P24	P24	AA10	
36	rx_hdluma(2)	K12	G12	G12	M27	M27	AA8	
37	rx_reset	A9	D16	D16	G31	G31	AL8	
38	rx_fpgavclk	H16	F21	F21	F33	F33	AP9	
61	rx_chromaluma(9)	A11	D20	D20	H34	H34	AB10	
62	rx_chromaluma(7)	C11	H20	H20	K33	K33	AB7	
63	rx_chromaluma(8)	A12	C20	C20	H33	H33	AB11	
64	rx_chromaluma(6)	C12	J20	J20	K32	K32	AB8	
65	rx_chromaluma(5)	B11	K17	K17	P27	P27	AJ6	
66	rx_chromaluma(3)	B13	F15	F15	K34	K34	AD7	
67	rx_chromaluma(4)	B12	L17	L17	N27	N27	AJ7	
68	rx_chromaluma(2)	B14	E15	E15	J34	J34	AE7	
69	rx_chromaluma(1)	D12	J17	J17	N30	N30	AH7	
71	rx_chromaluma(0)	D13	H17	H17	N29	N29	AG7	
74	tx_sel(1)	J14	L16	L16	AA28	T23	AC10	
76	tx_sel(0)	J15	M16	M16	AA29	U23	AD10	
77	tx_sel(3)	K13	E17	E17	W24	R26	AE9	
78	tx_chromaluma(2)	C13	K16	K16	AA30	T25	AG10	
79	tx_sel(2)	K14	E18	E18	Y24	T26	AF9	
80	tx_chromaluma(3)	C14	J16	J16	AB30	T24	AF10	
81	tx_chromaluma(0)	K16	K19	K19	AE34	R29	AK8	
82	tx_chromaluma(6)	H14	H16	H16	AC28	N32	AG11	
83	tx_chromaluma(1)	K15	J19	J19	AE33	P29	AK9	
84	tx_chromaluma(7)	H15	G16	G16	AB28	P32	AF11	
85	tx_chromaluma(4)	G16	H19	H19	AC30	P31	AH10	
86	tx_hdluma(0)	F16	M17	M17	AD32	T31	AE11	
87	tx_chromaluma(5)	G17	G19	G19	AC29	P30	AJ10	
88	tx_hdluma(1)	F17	M18	M18	AE32	R31	AD11	
89	tx_fpgavclk	E16	K21	K21	AC32	R32	AE8	
90	tx_hdluma(4)	C16	C19	C19	AA24	V34	AH9	
92	tx_hdluma(5)	D17	D19	D19	AA23	V33	W7	

93	tx_chromaluma(8)	F13	E19	E19	AF34	T34	AN13	
94	tx_hdluma(8)	D18	E28	E28	AD29	U27	AE4	
95	tx_chromaluma(9)	G15	F19	F19	AF33	T33	AC8	
96	tx_hdluma(9)	C18	F28	F28	AE29	U26	AC3	
98	tx_hdluma(6)	G18	C29	C29	AE31	U31	Y9	
100	tx_hdluma(7)	G19	C28	C28	AF31	U30	W9	
101	tx_hdluma(2)	F18	H27	H27	AH34	U33	W11	
102	fpga_oscck	E18	J22	J22	AN22	AC28	AG1	
103	tx_hdluma(3)	F19	G27	G27	AJ34	U32	Y11	
106	tx_vclk	F22	L27	L27	H32	H32	AF18	
140	rx_refck	E22	D23	D23	AP27	AJ34	AF5	
142	osc_enab	B21	G24	G24	AJ29	AA29	AG6	
144	tx_refck	B22	H24	H24	AK29	AA28	AF6	
145	tx_iopins(0)	E26	H33	H33	AL21	AE34	AJ5	
147	tx_iopins(1)	F27	J33	J33	AK21	AE33	AK4	
149	tx_iopins(2)	J23	C32	C32	AK22	AG32	V4	
150	tx_iopins(4)	D22	K25	K25	AN30	AC30	AH5	
151	tx_iopins(3)	J24	C33	C33	AK23	AG33	V3	
152	tx_iopins(5)	D23	L25	L25	AP30	AC29	AG5	
153	tx_iopins(6)	E27	H34	H34	AP29	AD27	Y3	
154	tx_aux(0)	C22	E24	E24	AE27	Y24	Y1	
155	tx_iopins(7)	E28	G34	G34	AN29	AC27	Y2	
156	tx_aux(1)	C23	F24	F24	AF28	W24	W2	
157	tx_aux(2)	D29	E33	E33	AP26	AD29	AA1	
158	tx_aux(4)	B23	K23	K23	AL30	AD32	AA3	
159	tx_aux(3)	C29	D33	D33	AP25	AE29	AB1	
160	tx_aux(5)	B24	L23	L23	AM30	AE32	AB3	
161	tx_aux(6)	G23	C24	C24	AH28	AC32	AC2	
162	tx_aux(8)	F23	G30	G30	AH27	AE31	AD2	
163	tx_aux(7)	G22	D24	D24	AH29	AC33	AD1	
164	tx_aux(9)	F24	H30	H30	AJ27	AF31	AE2	
176	tx_anc_ctrlbar	D26	M30	M30	AL26	AK33	AN2	
177	tx_reset	B32	E32	E32	AM25	AH30	AL3	
178	tx_rd_wrbar	K21	J23	J23	AM23	AL31	AN3	
179	tx_sdsel	C33	F32	F32	AN25	AJ30	AM2	
180	tx_aclk	K20	H23	H23	AL23	AM31	AM3	

7. BoardLayout



RevisionHistory

Date	Revision	Comment
Oct-2006	-	Initialdraft
	1.0	Firstrelease.
Nov06	1.1	Added def for Tx clock pin to serialiser