User Manual
For the XRM-RS422
Alpha Data Part Number AD01134

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1 Introduction

The XRM-RS422 is a custom XRM for interfacing to standard RS422 signals. The XRM-RS422 has only inputs.

1.1 General Specification

50 pin SCSI type connector, female
Differential data inputs, RS422 standard

- 19 data

LVTTL Level Signals

- Input : 1 clock @ 80 MHz
- Output : 1 sync pulse

2 Environmental Specification

Temperature	:	0 deg C to +55 deg C at maximum PMC dissipation
Humidity	:	TBD
Vibration	:	TBD
Reliability	:	1,000,000 hours

3 Mechanical Specification

3.1 XRM™ Compliance

The board shall comply with the Alpha Data XRM specification.

4 Electrical Specification

4.1 Power Requirements

Maximum +5V @ 0.5A
Maximum +3V3 @ 0.5A

4.2 JTAG

This XRM does not use JTAG capable components and therefore TDI should be connected directly to TDO.

4.3 XRM Interface

See separate specification of the XRM.

5 Functional Specifications

5.1 RS422

This XRM receives RS422 data from an external camera and converts it to single ended LVTTL. There is no specific skew specification from the customer but care should be taken to minimise it.

The XRM will use 5 x Texas AM26LV32D quad RS-422 receivers in 10x6mm SOIC. These devices use a 3V3 supply and have a low power requirement.

An alternative for higher speed is the Sipex SP26LV432CN, also in a 16 SOIC but with 50Mbps performance.

These parts do not contain termination resistors.

NOTE. These devices will have to be fitted on one side of the XRM due to the requirement for 0mm height on side 2.

5.2 TTL

5.2.1 CLKIN

The XRM receives a clock from an adjacent card in the PC, a National Instruments NI6602 counter timer. The clock is TTL level single ended and should be received using a device that can safely drive the FPGA at LVTTL levels.

5.2.2 Sync

The XRM generates a TTL level sync pulse to the NI6602. A TTL translator should be used to drive this signal from the XRM to protect the FPGA.

6 Mechanical

The XRM shall be as shown in the drawing below. It should be noted that where through hole components are used these should be cropped on the non-component side to 0mm height.

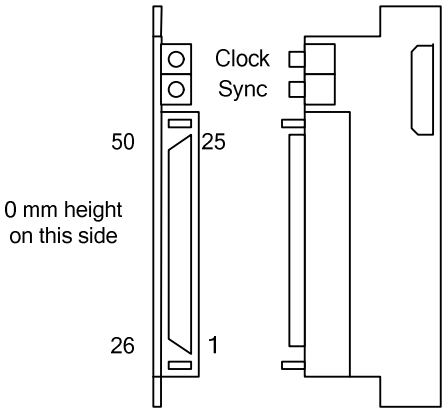


Figure 1 Basic Mechanical Outline

6.1 Pinout – NI6602 Interface

There are two signals – Clock and Sync - shall use MCX 50 Ohm connectors for use with coaxial cabling. See RS Catalogue 245-5159.

6.2 Pinout – RS422

The XRM uses a 50 pin connector with the following pin-out for the RS422 interface. An AMP 787394-5 is a potential candidate.

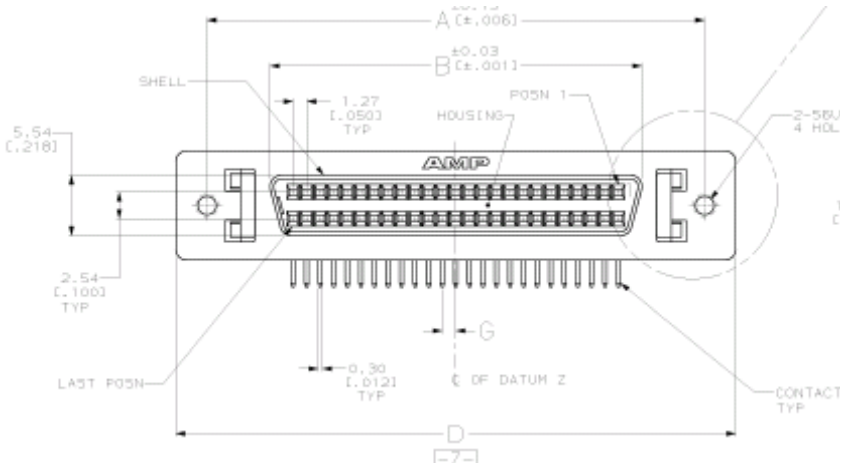


Figure 2 RS422 Connector Mechanical

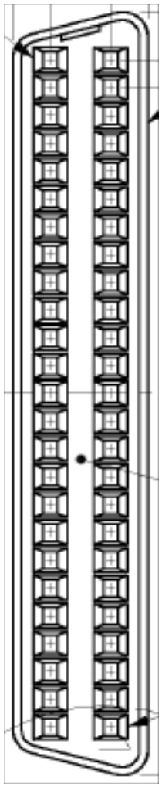
TTL_GND	50		25	TTL_GND
P1	49		24	N1
P2	48		23	N2
P3	47		22	N3
P4	46		21	N4
P5	45		20	N5
P6	44		19	N6
P7	43		18	N7
P8	42		17	N8
P9	41		16	N9
P10	40		15	N10
P11	39		14	N11
P12	38		13	N12
P13	37		12	N13
P14	36		11	N14
P15	35		10	N15
P16	34		9	N16
TTL_GND	33		8	TTL_GND
TTL_GND	32		7	TTL_GND
CLK_P	31		6	CLK_N
TTL_GND	30		5	TTL_GND
FSYNC_P	29		4	FSYNC_N
TTL_GND	28		3	TTL_GND
LSYNC_P	27		2	LSYNC_N
TTL_GND	26		1	TTL_GND

Figure 3 RS422 Interface Pin-Out

RS422 Pair	RS422	XPL FPGA Pin
P9/N9	D9	C7
P7/N7	D7	D7
P5/N5	D5	D8
P3/N3	D3	C8
P4/N4	D4	A8
P8/N8	D8	B8
P11/N11	D11	D10
P2/N2	D2	E10
P1/N1	D1	C9
P10/N10	D10	B9
P12/N12	D12	D11
P14/N14	D14	E11
P13/N13	D13	C10
P15/N15	D15	C11
P16/N16	D16	D13
P6/N6	D6	C13
FSYNC_P/FSYNC_N	FSYNC	D14
LSYNC_P/LSYNC_N	LSYNC	E14
CLK_P/CLK_N	CLK	C15

7 Change History

Date	New Version	Change Summary
24-11-05	1.0	Initial version