



ALPHA DATA

ADM-VA740 User Manual

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1 Introduction

The ADM-VA740 is a 3U VPX module. It includes an AMD Versal Premium device.

1.1 Key Features

Key Features

- 3U VPX Form Factor.
- Conduction cooled.
- Compatible with OpenVPX 14.8.7-n slot profile.
- Supports optional Alpha Data Optical Mezzanine cards.
- AMD Versal Premium VP1402 device in the VSVA3340 package.
- 3x banks of LPDDR4 memory.

1.2 References & Specifications

| | |
|----------------|--|
| ANSI/VITA 46.0 | <i>VPX Baseline Standard</i> , October 2007, VITA, ISBN 1-885731-44-2 |
| ANSI/VITA 47.0 | <i>Construction, Safety and Quality for Plug-In Modules Standard</i> , April 2019, VITA, ISBN 978-1-948739-08-5 |
| ANSI/VITA 48.0 | <i>Mechanical Specification for Microcomputers using Ruggedized Enhanced Design Implementation</i> , July 2020, VITA, ISBN 978-1-948739-20-7 |
| ANSI/VITA 65.0 | <i>OpenVPX™ System Specification</i> , June 2010, VITA, ISBN 1-885731-58-2 |
| ANSI/VITA 66.0 | <i>Optical Interconnect on VPX - Base Standard</i> , July 2016, VITA, ISBN 1-885731-90-6 |
| AMD DS959 | <i>Versal Premium Series Data Sheet: DC and AC Switching Characteristics</i> , June 2024, AMD |
| AMD AM002 | <i>Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual</i> , October 2023, AMD |
| AMD AM010 | <i>Versal Adaptive SoC SelectIO Resources Architecture Manual</i> , March 2024, AMD |
| AMD AM011 | <i>Versal Adaptive SoC Technical Reference Manual</i> , October 2023, AMD |
| AMD AM017 | <i>Versal ACAP GTM Transceivers Architecture Manual</i> , April 2022, AMD |
| AMD XAPP1375 | <i>Simplified Power Sequencing</i> , August 2024, AMD |
| AMD UG863 | <i>Versal Adaptive SoC PCB Design User Guide</i> , April 2024, AMD |
| AMD UG1304 | <i>Versal ACAP System Software Developers Guide</i> , October 2021, AMD |

Table 1 : References

1.3 Order Code

Order Code: **ADM-VA740**

See the https://alpha-data.com/xml//product_datasheets/adm-va740_v1.0.pdf datasheet[®] for complete ordering options.



Figure 1 : ADM-VA740

1.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products.

Please contact sales@alpha-data.com to obtain a quote and start your project today.

2 Installation

2.1 Hardware Installation

2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:



- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2 Hardware Installation

2.2.1 System Requirements

The ADM-VA740 is a 3U VPX platform featuring the AMD Versal Premium XCVP1402 Adaptable SoC.

2.2.2 Cooling Requirements

The power dissipation of the board is highly dependent on the Adaptive SoC application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with AMD power estimation tools to determine the approximate current requirements for each power rail.

The board is supplied with a conduction cooled heatsink. It is the users responsibility to ensure the metalwork is appropriate for conduction cooled applications.

3 Board Information

3.1 Physical Specifications

The ADM-VA740 complies with VITA48.2 (3U / 160mm VPX).

| Description | Measure |
|-------------------------------|-----------|
| Total Dy | 100.0 mm |
| Total Dx | 160.0 mm |
| PCB Dx | 157.70 mm |
| Total Dz | 23.42 mm |
| Circuit assembly weight | TBD grams |
| Total weight (with heat sink) | TBD grams |

Table 2 : Mechanical Dimensions

3.2 Chassis Requirements

3.2.1 Mechanical Requirements

A 3U VPX rack is required for mechanical compatibility.

3.2.2 Power Requirements

The ADM-VA740 is primarily powered via the +12V VPX power rail. The majority of internal power rails are generated from this rail.

The ADM-VA740 is capable of drawing up to 15A on the +12V VPX power rail.

The ADM-VA740 also requires the presence of a +3.3V_AUX auxiliary power rail, used to power the ACAP PMC, ACAP LPD, and on-board system monitoring and reset circuitry.

The ADM-VA740 is capable of drawing up to 1A on the +3.3V_AUX power rail.

Power consumption estimation requires the use of the AMD XPE spreadsheet (www.xilinx.com/products/technology/power/xpe.html) and a power estimator tool available from Alpha Data. Please contact support@alpha-data.com to obtain this tool.

The power available to the rails calculated using XPE are as follows:

| Voltage | Source Name | Current Capability |
|---------|--|--------------------|
| 0.80 | VCC_INT + VCC_PSFP | 80A |
| 0.80 | VCC_SOC + VCC_IO + VCC_RAM + VCCINT_GT | 40A |
| 0.92 | MGTAVCC | 15A |
| 1.2 | MGTAVTT | 10A |
| 1.1 | VCCO + LPDDR4 | 6A |
| 1.5 | VCCAUX | 5A |

Table 3 : Available Power By Rail

4 Functional Description

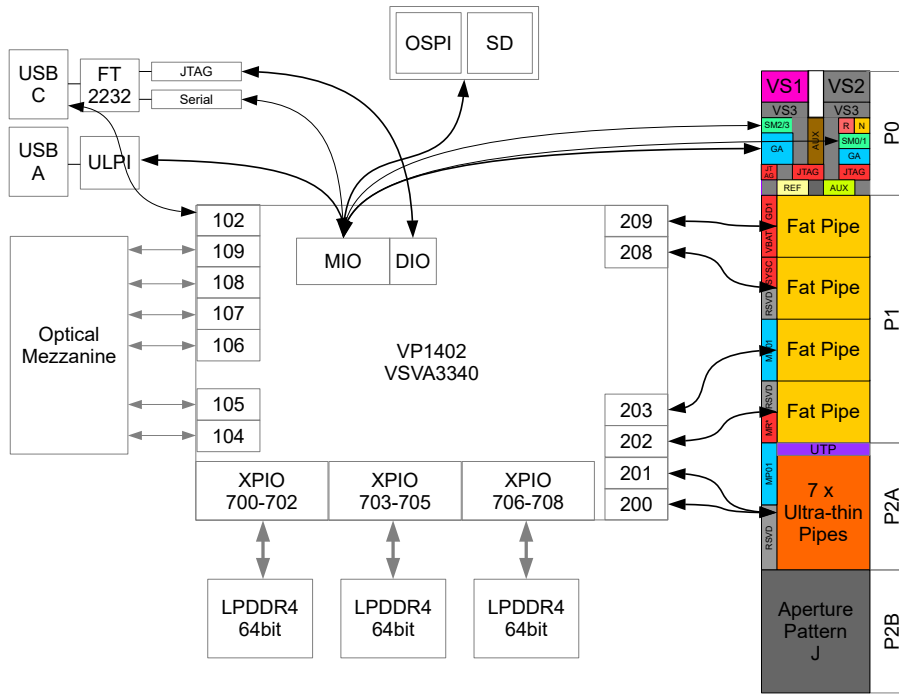


Figure 2 : Bank Diagram

4.1 Switch Definitions

| Comp. Ref. | Function | ON State | Off State |
|------------|-------------|------------------------------------|-----------------------------------|
| SW1-1 | ACAP MODE0 | MODE0=LOW | MODE0=HIGH |
| SW1-2 | ACAP MODE1 | MODE1=LOW | MODE1=HIGH |
| SW1-3 | ACAP MODE2 | MODE2=LOW | MODE2=HIGH |
| SW1-4 | ACAP MODE3 | MODE3=LOW | MODE3=HIGH |
| SW1-5 | JTAG select | Factory Use Only | Normal Operation |
| SW1-6 | Power Mode | +12V VPX derived supplies disabled | +12V VPX derived supplies enabled |
| SW1-7 | User Switch | Normal Operation | Normal Operation |
| SW1-8 | POR_B | ACAP held in reset | ACAP reset released |

Table 4 : Switch Definitions (SW1)

4.2 LED Definitions

| Comp. Ref. | Function | ON State | Off State |
|-------------|------------------------|------------------|----------------------|
| D12 (Red) | PS Error | PS Error | Normal Operation |
| D13 (Green) | Adaptive SoC (PL) Done | PL is configured | PL is not configured |

Table 5 : Status LED Definitions

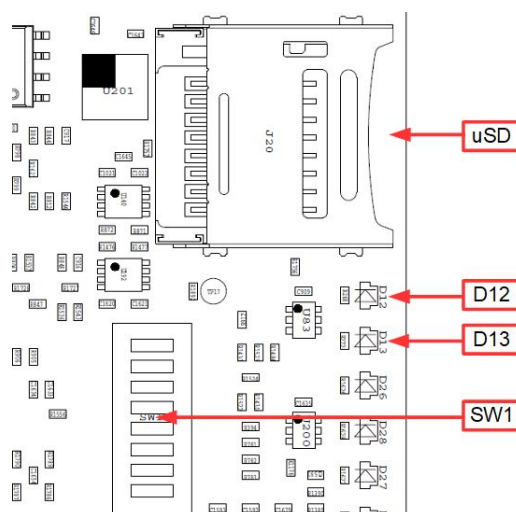


Figure 3 : Switches and LEDs

4.3 JTAG Interface

4.3.1 On-board Interface

The ACAP is the only on-board device in the JTAG chain.

The ACAP can be accessed over JTAG from the front USB-C connector.

Alternatively, JTAG access is possible from the backplane P0 interface (3.3V signal levels) when the USB-C interface is not in use.

4.4 ACAP

4.4.1 I/O Bank Voltages

The ACAP I/O is arranged in banks, each with its own supply pins. The bank numbers, their voltage, and function are shown below.

| I/O Banks | Voltage | Purpose |
|----------------------|---------|-------------------------|
| 500 (DIO) | 1.8V | OSPI, ULPI |
| 501 (MIO) | 3.3V | SDIO and misc. signals. |
| 502 (MIO) | 3.3V | misc. signals |
| 503 (MIO) | 3.3V | JTAG |
| 612 (HDIO) | 3.3V | misc. signals |
| 613 (HDIO) | 3.3V | misc. signals |
| 700, 701, 702 (HDIO) | 1.1V | LPDDR4 |
| 703, 704, 705 (HDIO) | 1.1V | LPDDR4 |
| 706, 707, 708 (HDIO) | 1.1V | LPDDR4 |

Table 6 : Target FPGA I/O Banks

4.4.2 ACAP Processing System

4.4.2.1 Flash Memory

A 2Gb Flash memory (Micron mt35xu02gcba1g12-osit) is connected to the ACAP, and can be used to store configuration bitstreams.

4.4.2.2 SD Card

A micro SD card can be inserted into J20 and used to store configuration bitstreams.

The SD card interface uses SD_eMMC1, SD v2.0 Boot, interface of PMC MIO Bank 501.

4.4.2.3 USB 2.0

An USB peripheral device can be inserted into J15.

The USB interface uses the USB 2.0 interface of PMC MIO Bank 500.

4.4.2.4 Boot Modes

| MODE3 (SW1-4) | MODE2 (SW1-3) | MODE1 (SW1-2) | MODE0 (SW1-1) | Boot Mode |
|------------------|------------------|------------------|------------------|-------------------|
| ON | ON | ON | ON | JTAG |
| OFF | ON | ON | ON | Octal SPI |
| ON | OFF | ON | OFF | SD Flash - SD 2.0 |

Table 7 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

4.4.3 ACAP Programmable Logic

4.4.3.1 ACAP MGT Links

| Links | Width | Quad | Quad Type |
|--------|-------|------|-----------|
| OMFP0 | 4 | 104 | GTM |
| OMFP1 | 4 | 105 | GTM |
| OMFP2 | 4 | 106 | GTM |
| OMFP3 | 4 | 107 | GTM |
| OMFP4 | 4 | 108 | GTM |
| OMFP5 | 4 | 109 | GTM |
| CPUTPs | 4 | 200 | GTM |
| CPUTPs | 4 | 201 | GTM |
| DPFP03 | 4 | 202 | GTM |
| DPFP02 | 4 | 203 | GTM |
| DPFP01 | 4 | 208 | GTM |
| DSFP01 | 4 | 209 | GTM |

Table 8 : MGT Links

For MGT Clocking, please refer to [Clocks](#).

4.4.3.2 Memory Interfaces

4.4.3.2.1 LPDDR4 SDRAM

The ADM-VA740 has three banks of LPDDR4 SDRAM.

Each bank consists of two 32-bit wide memory devices in parallel.

Micron MT53E1G32D2FW-046 IT are fitted as standard to provide 8GB per bank.

The memory banks are arranged for compatibility with the AMD Versal Memory Controllers in the XPIO banks.

4.5 Clocks

The clock routing on the ADM-VA740 is illustrated below.

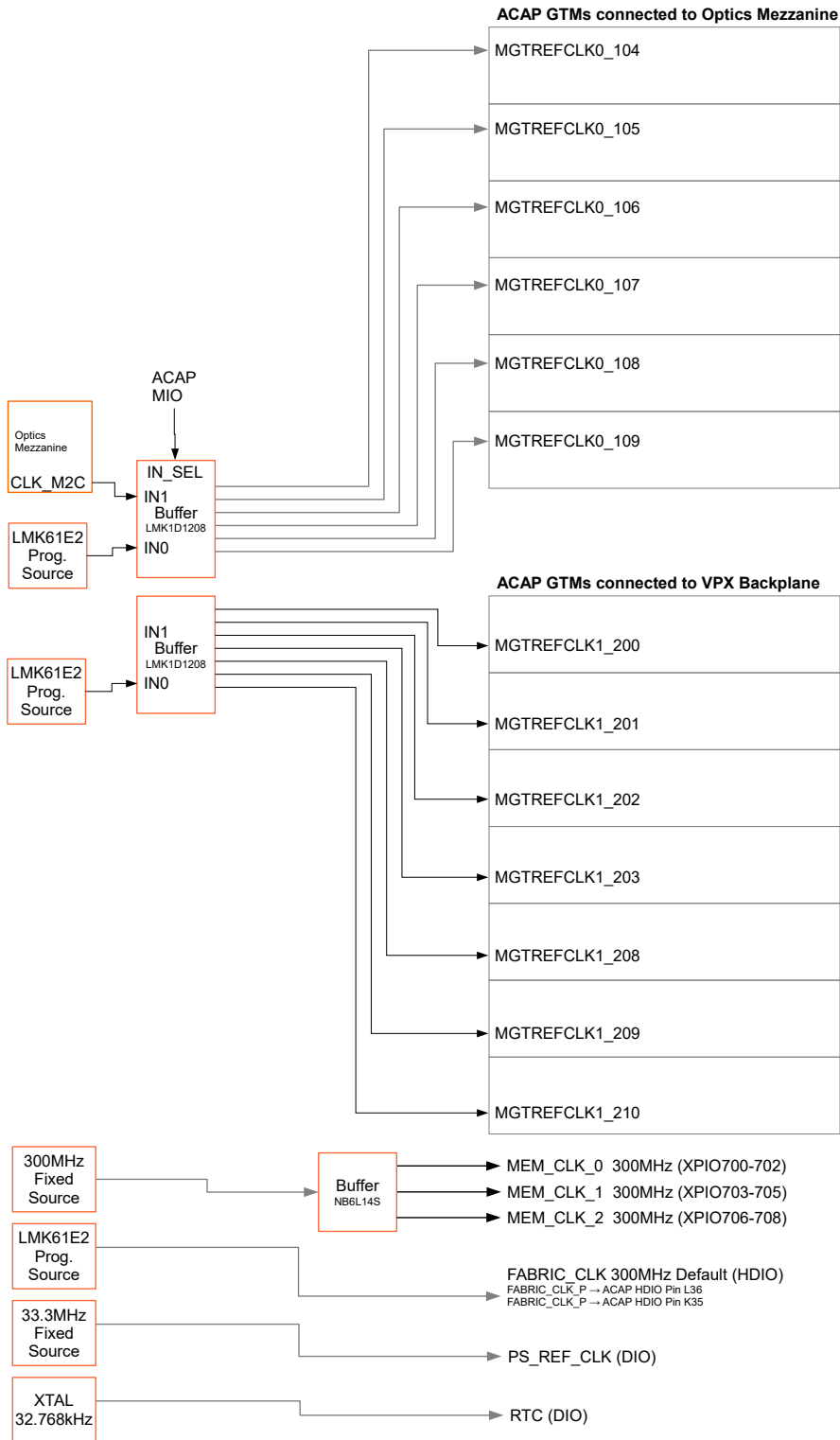


Figure 4 : Clocks

4.6 VPX P0 Interface

4.6.1 SYSRESET*

A buffered version of SYSRESET* connects to ACAP LPD_MIO25.

A buffered version of SYSRESET* also connects to ACAP HDIO Pin M38 (LVCMOS33).

4.6.2 NVMRO

A buffered version of NVMRO connects to ACAP HDIO Pin N38 (LVCMOS33).

4.6.3 GDiscrete1

A buffered version of GDiscrete1 connects to ACAP HDIO Pin N39 (LVCMOS33).

4.6.4 Global Address

A buffered version of GA0 connects to ACAP PMC_MIO49.

A buffered version of GA1 connects to ACAP PMC_MIO48.

A buffered version of GA2 connects to ACAP PMC_MIO47.

A buffered version of GA3 connects to ACAP PMC_MIO46.

A buffered version of GA4 connects to ACAP PMC_MIO45.

A buffered version of GAP connects to ACAP PMC_MIO44.

To read GA3, GA4, GDiscrete1, or to use MP01, the ACAP must drive PMC_MIO37 LOW.

4.6.5 MaskableReset

A buffered version of MaskableReset* connects to ACAP HDIO Pin M39 (LVCMOS33).

4.6.6 REF_CLK

A buffered version of REF_CLK+ connects to ACAP HDIO Pin L40 (LVDS_25).

A buffered version of REF_CLK- connects to ACAP HDIO Pin K40 (LVDS_25).

REF_CLK is terminated on the PCB.

4.6.7 AUX_CLK

A buffered, single ended, version of AUX_CLK connects to ACAP HDIO Pin L39 (LVCMOS33).

4.6.8 I2C

4.6.8.1 Primary I2C

The Primary I2C Interface SM0/SM1 connects to ACAP LPD_MIO22/LPD_MIO23.

The Primary I2C Interface is buffered using an Analog Devices LTC4307 device.

The buffer enable pin is connected to the ACAP LPD_MIO4.

The buffer ready pin is connected to the ACAP LPD_MIO5.

4.6.8.2 Secondary I2C

The Secondary I2C Interface SM2/SM3 connects to ACAP LPD_MIO20/LPD_MIO21.

The Secondary I2C Interface is buffered using an Analog Devices LTC4307 device.

The buffer enable pin is connected to the ACAP LPD_MIO6.

The buffer ready pin is connected to the ACAP LPD_MIO7.

4.7 VPX P1 Interfaces

4.7.1 HSSIO

Refer to the ACAP MGT Links section for details of the HSSIO connections.

4.7.2 VBAT

VBAT connects to the ACAP VCC_BATT pin via an LDO.

4.7.3 MP01

MP01 connects to the ACAP via buffering.

To read GA3, GA4, GDiscrete1, or to use MP01, the ACAP must drive PMC_MIO37 LOW.

MP01_TD connects to ACAP LPD_MIO17.

MP01_RD connects to ACAP LPD_MIO16.

4.8 VPX P2 Interfaces

4.8.1 HSSIO

Refer to the ACAP MGT Links section for details of the HSSIO connections.

4.8.2 MP02

MP02 connects to the ACAP via buffering.

To use MP01, the ACAP must drive HDIO Pin M41 LOW (LVCMOS33).

MP02_TD connects to ACAP HDIO Pin L42 (LVCMOS33).

MP02_RD connects to ACAP HDIO Pin M42 (LVCMOS33).

4.9 Optical Mezzanine Site

The ADM-VA740 includes an optical mezzanine site, please refer to the bank diagram for an overview of the connections.

Optical mezzanine cards are in an Alpha Data proprietary form factor. Please contact sales@alpha-data.com for more information.

4.9.1 Optical Mezzanine Site

The Optical Mezzanine site allows the connection of custom form factor boards intended to host optical modules.

4.9.1.1 Connectors

The Optical Mezzanine site consists of J21 and J22.

4.9.1.2 ACAP HSSIO

Six ACAP GTM transceiver quads are connected to the Optical Mezzanine Site.

Refer to ACAP MGT Links section for further details.

4.9.1.3 I2C

The I2C interfaces of the off-board optical modules connect to the ACAP HDIO via buffering.

SCL connects to ACAP HDIO Pin N33 (LVCMOS33).

SDA connects to ACAP HDIO Pin M32 (LVCMOS33).

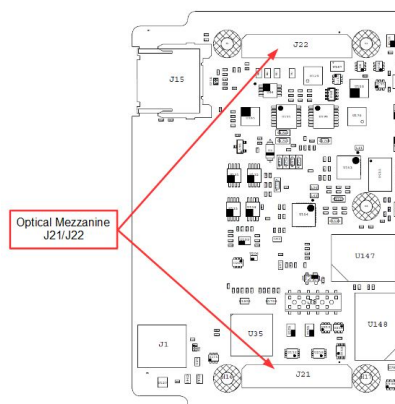


Figure 5 : Optical Mezzanine Connectors

4.10 System Monitoring

The ADM-VA740 hardware includes on-board circuitry to support system monitoring.

This includes the monitoring of the voltage levels of external power supply rails and the current drawn from them.

The system monitoring circuitry also supports the monitoring of the status of the on-board voltage regulators.

Additionally, the PCB temperature is monitored in key locations.

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Appendix A: LPDDR4 Pinout

| Pin Number | Signal Name |
|------------|-------------------------|
| BF12 | REFCLK_MEM0_P |
| BG11 | REFCLK_MEM0_N |
| BV11 | LPDDR4_0_CH1_CK_C_A[0] |
| BU11 | LPDDR4_0_CH1_CK_T_A[0] |
| BT15 | LPDDR4_0_CH1_DQ_A[6] |
| BR15 | LPDDR4_0_CH1_DQ_A[7] |
| BT17 | LPDDR4_0_CH1_DQ_A[4] |
| BR17 | LPDDR4_0_CH1_DQ_A[5] |
| BL12 | LPDDR4_0_CH1_CK_C_B[0] |
| BL11 | LPDDR4_0_CH1_CK_T_B[0] |
| BM14 | LPDDR4_0_CH1_CA_B[3] |
| BL13 | LPDDR4_0_CH1_CA_B[4] |
| BM15 | LPDDR4_0_CH1_CA_B[1] |
| BL15 | LPDDR4_0_CH1_CA_B[0] |
| BN16 | LPDDR4_0_CH1_CKE_B[0] |
| BM17 | LPDDR4_0_CH1_CKE_B[1] |
| BN11 | LPDDR4_0_CH1_CA_B[2] |
| BM11 | LPDDR4_0_CH1_CA_B[5] |
| BJ13 | LPDDR4_0_CH1_DQS_C_B[0] |
| BJ12 | LPDDR4_0_CH1_DQS_T_B[0] |
| BJ16 | LPDDR4_0_CH1_DQ_B[5] |
| BJ15 | LPDDR4_0_CH1_DQ_B[7] |
| BV13 | LPDDR4_0_CH1_CA_A[5] |
| BU12 | LPDDR4_0_CH1_CA_A[4] |
| BL17 | LPDDR4_0_CH1_DQ_B[3] |
| BK17 | LPDDR4_0_CH1_DQ_B[2] |
| BL16 | LPDDR4_0_CH1_CS_B[1] |
| BK15 | LPDDR4_0_CH1_DMI_B[0] |
| BK14 | LPDDR4_0_CH1_DQ_B[1] |
| BK13 | LPDDR4_0_CH1_DQ_B[0] |
| BL10 | LPDDR4_0_CH1_DQ_B[4] |
| BK10 | LPDDR4_0_CH1_DQ_B[6] |
| BU14 | LPDDR4_0_CH1_CS_A[1] |
| BU13 | LPDDR4_0_CH1_CKE_A[0] |

Table 9 : Bank 0 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BV15 | LPDDR4_0_CH1_CKE_A[1] |
| BV14 | LPDDR4_0_CH1_CS_A[0] |
| BU16 | LPDDR4_0_CH1_CA_A[0] |
| BT16 | LPDDR4_0_CH1_CA_A[1] |
| BV16 | LPDDR4_0_CH1_CA_A[2] |
| BU17 | LPDDR4_0_CH1_CA_A[3] |
| BT11 | LPDDR4_0_CH1_CS_B[0] |
| BR10 | LPDDR4_0_CH1_DMI_A[0] |
| BT12 | LPDDR4_0_CH1_DQ_A[2] |
| BR12 | LPDDR4_0_CH1_DQ_A[3] |
| BR13 | LPDDR4_0_CH1_DQ_A[1] |
| BP13 | LPDDR4_0_CH1_DQ_A[0] |
| BT14 | LPDDR4_0_CH1_DQS_C_A[0] |
| BR14 | LPDDR4_0_CH1_DQS_T_A[0] |
| BH4 | LPDDR4_0_CH0_CS_B[0] |
| BH5 | LPDDR4_0_CH0_DMI_B[1] |
| BG6 | LPDDR4_0_CH0_DQ_A[11] |
| BF6 | LPDDR4_0_CH0_DQ_A[10] |
| BJ5 | LPDDR4_0_CH0_DQ_A[13] |
| BH6 | LPDDR4_0_CH0_DQ_A[12] |
| BH13 | LPDDR4_0_CH0_CK_C_B[0] |
| BH14 | LPDDR4_0_CH0_CK_T_B[0] |
| BF13 | LPDDR4_0_CH0_CA_B[4] |
| BF14 | LPDDR4_0_CH0_CA_B[5] |
| BE13 | LPDDR4_0_CH0_CA_B[1] |
| BD14 | LPDDR4_0_CH0_CKE_B[0] |
| BD13 | LPDDR4_0_CH0_CKE_B[1] |
| BC13 | LPDDR4_0_CH0_CA_B[0] |
| BG12 | LPDDR4_0_CH0_CA_B[2] |
| BG13 | LPDDR4_0_CH0_CA_B[3] |
| BC17 | LPDDR4_0_CH0_CK_C_A[0] |
| BB17 | LPDDR4_0_CH0_CK_T_A[0] |
| BC16 | LPDDR4_0_CH0_CA_A[5] |
| BD17 | LPDDR4_0_CH0_CA_A[4] |
| BG3 | LPDDR4_0_CH0_DQ_B[9] |
| BG4 | LPDDR4_0_CH0_DQ_B[10] |

Table 9 : Bank 0 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BC15 | LPDDR4_0_CH0_CKE_A[1] |
| BB15 | LPDDR4_0_CH0_CKE_A[0] |
| BE15 | LPDDR4_0_CH0_CS_A[1] |
| BD15 | LPDDR4_0_CH0_CA_A[2] |
| BG15 | LPDDR4_0_CH0_CA_A[0] |
| BF15 | LPDDR4_0_CH0_CA_A[1] |
| BH15 | LPDDR4_0_CH0_CA_A[3] |
| BG16 | LPDDR4_0_CH0_CS_A[0] |
| BE11 | LPDDR4_0_CH1_RESET_N[0] |
| BE12 | LPDDR4_0_CH0_RESET_N[0] |
| BJ3 | LPDDR4_0_CH0_DQ_B[14] |
| BH3 | LPDDR4_0_CH0_DQ_B[8] |
| BF1 | LPDDR4_0_CH0_DQS_C_B[1] |
| BG2 | LPDDR4_0_CH0_DQS_T_B[1] |
| BH1 | LPDDR4_0_CH0_DQ_B[15] |
| BG1 | LPDDR4_0_CH0_DQ_B[12] |
| BJ1 | LPDDR4_0_CH0_DQ_B[13] |
| BJ2 | LPDDR4_0_CH0_DQ_B[11] |
| BG8 | LPDDR4_0_CH0_DQS_C_A[1] |
| BH9 | LPDDR4_0_CH0_DQS_T_A[1] |
| BJ8 | LPDDR4_0_CH0_DQ_A[9] |
| BJ9 | LPDDR4_0_CH0_DQ_A[8] |
| BJ6 | LPDDR4_0_CH0_DQ_A[14] |
| BJ7 | LPDDR4_0_CH0_DQ_A[15] |
| BH7 | LPDDR4_0_CH0_CS_B[1] |
| BG7 | LPDDR4_0_CH0_DMI_A[1] |
| BK4 | LPDDR4_0_CH0_DQS_C_B[0] |
| BK5 | LPDDR4_0_CH0_DQS_T_B[0] |
| BR2 | LPDDR4_0_CH1_DQ_B[12] |
| BP2 | LPDDR4_0_CH1_DQ_B[13] |
| BP1 | LPDDR4_0_CH1_DQ_B[14] |
| BN1 | LPDDR4_0_CH1_DQ_B[15] |
| BM9 | LPDDR4_0_CH0_DQS_C_A[0] |
| BL9 | LPDDR4_0_CH0_DQS_T_A[0] |
| BL8 | LPDDR4_0_CH0_DQ_A[0] |
| BK8 | LPDDR4_0_CH0_DQ_A[3] |

Table 9 : Bank 0 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BM7 | LPDDR4_0_CH0_DQ_A[4] |
| BL7 | LPDDR4_0_CH0_DQ_A[2] |
| BP7 | LPDDR4_0_CH0_DMI_A[0] |
| BP6 | LPDDR4_0_CH0_DQ_A[7] |
| BN6 | LPDDR4_0_CH0_DQ_A[6] |
| BM6 | LPDDR4_0_CH0_DQ_A[5] |
| BL6 | LPDDR4_0_CH0_DQ_A[1] |
| BT10 | LPDDR4_0_CH1_DMI_A[1] |
| BV9 | LPDDR4_0_CH1_DQ_A[9] |
| BV10 | LPDDR4_0_CH1_DQ_A[8] |
| BL4 | LPDDR4_0_CH0_DQ_B[1] |
| BL5 | LPDDR4_0_CH0_DQ_B[3] |
| BT9 | LPDDR4_0_CH1_DQ_A[15] |
| BR9 | LPDDR4_0_CH1_DQ_A[12] |
| BT7 | LPDDR4_0_CH1_DQS_C_A[1] |
| BR8 | LPDDR4_0_CH1_DQS_T_A[1] |
| BV8 | LPDDR4_0_CH1_DQ_A[10] |
| BU8 | LPDDR4_0_CH1_DQ_A[11] |
| BU6 | LPDDR4_0_CH1_DQ_A[13] |
| BU7 | LPDDR4_0_CH1_DQ_A[14] |
| BM3 | LPDDR4_0_CH0_DQ_B[0] |
| BM4 | LPDDR4_0_CH0_DQ_B[2] |
| BM2 | LPDDR4_0_CH0_DMI_B[0] |
| BL1 | LPDDR4_0_CH0_DQ_B[6] |
| BL2 | LPDDR4_0_CH0_DQ_B[7] |
| BK2 | LPDDR4_0_CH0_DQ_B[5] |
| BK3 | LPDDR4_0_CH0_DQ_B[4] |
| BN4 | LPDDR4_0_CH1_DQS_C_B[1] |
| BN5 | LPDDR4_0_CH1_DQS_T_B[1] |
| BR3 | LPDDR4_0_CH1_DQ_B[9] |
| BR4 | LPDDR4_0_CH1_DQ_B[8] |
| BU4 | LPDDR4_0_CH1_DQ_B[11] |
| BT4 | LPDDR4_0_CH1_DQ_B[10] |
| BN3 | LPDDR4_0_CH1_DMI_B[1] |

Table 9 : Bank 0

| Pin Number | Signal Name |
|------------|-------------------------|
| BK21 | REFCLK_MEM1_P |
| BK22 | REFCLK_MEM1_N |
| BT22 | LPDDR4_1_CH0_CS_B[0] |
| BR22 | LPDDR4_1_CH0_DMI_B[1] |
| BT19 | LPDDR4_1_CH0_DQ_A[13] |
| BR19 | LPDDR4_1_CH0_DQ_A[12] |
| BR18 | LPDDR4_1_CH0_DQ_A[9] |
| BP18 | LPDDR4_1_CH0_DQ_A[10] |
| BJ17 | LPDDR4_1_CH0_CK_C_B[0] |
| BH18 | LPDDR4_1_CH0_CK_T_B[0] |
| BH19 | LPDDR4_1_CH0_CA_B[4] |
| BG20 | LPDDR4_1_CH0_CA_B[5] |
| BH22 | LPDDR4_1_CH0_CA_B[1] |
| BH21 | LPDDR4_1_CH0_CKE_B[0] |
| BK19 | LPDDR4_1_CH0_CKE_B[1] |
| BJ19 | LPDDR4_1_CH0_CA_B[0] |
| BL19 | LPDDR4_1_CH0_CA_B[2] |
| BK18 | LPDDR4_1_CH0_CA_B[3] |
| BF18 | LPDDR4_1_CH0_CK_C_A[0] |
| BE17 | LPDDR4_1_CH0_CK_T_A[0] |
| BE20 | LPDDR4_1_CH0_CA_A[5] |
| BE19 | LPDDR4_1_CH0_CA_A[4] |
| BT21 | LPDDR4_1_CH0_DQ_B[13] |
| BT20 | LPDDR4_1_CH0_DQ_B[12] |
| BF22 | LPDDR4_1_CH0_CKE_A[1] |
| BE22 | LPDDR4_1_CH0_CKE_A[0] |
| BG21 | LPDDR4_1_CH0_CS_A[1] |
| BF21 | LPDDR4_1_CH0_CA_A[2] |
| BG19 | LPDDR4_1_CH0_CA_A[0] |
| BF19 | LPDDR4_1_CH0_CA_A[1] |
| BH17 | LPDDR4_1_CH0_CA_A[3] |
| BG17 | LPDDR4_1_CH0_CS_A[0] |
| BL21 | LPDDR4_1_CH1_RESET_N[0] |
| BL20 | LPDDR4_1_CH0_RESET_N[0] |
| BU19 | LPDDR4_1_CH0_DQ_B[9] |
| BU18 | LPDDR4_1_CH0_DQ_B[11] |

Table 10 : Bank 1 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BU22 | LPDDR4_1_CH0_DQS_C_B[1] |
| BU21 | LPDDR4_1_CH0_DQS_T_B[1] |
| BV21 | LPDDR4_1_CH0_DQ_B[14] |
| BV20 | LPDDR4_1_CH0_DQ_B[15] |
| BV19 | LPDDR4_1_CH0_DQ_B[8] |
| BV18 | LPDDR4_1_CH0_DQ_B[10] |
| BM19 | LPDDR4_1_CH0_DQS_C_A[1] |
| BM18 | LPDDR4_1_CH0_DQS_T_A[1] |
| BN20 | LPDDR4_1_CH0_DQ_A[11] |
| BN19 | LPDDR4_1_CH0_DQ_A[8] |
| BP21 | LPDDR4_1_CH0_DQ_A[15] |
| BN21 | LPDDR4_1_CH0_DQ_A[14] |
| BR20 | LPDDR4_1_CH0_CS_B[1] |
| BP20 | LPDDR4_1_CH0_DMI_A[1] |
| BN24 | LPDDR4_1_CH0_DQS_C_B[0] |
| BM23 | LPDDR4_1_CH0_DQS_T_B[0] |
| BU27 | LPDDR4_1_CH1_DQ_B[12] |
| BT27 | LPDDR4_1_CH1_DQ_B[13] |
| BV26 | LPDDR4_1_CH1_DQ_B[15] |
| BU26 | LPDDR4_1_CH1_DQ_B[14] |
| BE23 | LPDDR4_1_CH0_DQS_C_A[0] |
| BD24 | LPDDR4_1_CH0_DQS_T_A[0] |
| BG24 | LPDDR4_1_CH0_DQ_A[5] |
| BF24 | LPDDR4_1_CH0_DQ_A[3] |
| BH23 | LPDDR4_1_CH0_DQ_A[1] |
| BG23 | LPDDR4_1_CH0_DQ_A[2] |
| BH25 | LPDDR4_1_CH0_DMI_A[0] |
| BJ25 | LPDDR4_1_CH0_DQ_A[7] |
| BJ24 | LPDDR4_1_CH0_DQ_A[6] |
| BK23 | LPDDR4_1_CH0_DQ_A[4] |
| BJ23 | LPDDR4_1_CH0_DQ_A[0] |
| BD26 | LPDDR4_1_CH1_DMI_A[1] |
| BE26 | LPDDR4_1_CH1_DQ_A[9] |
| BE25 | LPDDR4_1_CH1_DQ_A[8] |
| BN25 | LPDDR4_1_CH0_DQ_B[6] |
| BM25 | LPDDR4_1_CH0_DQ_B[7] |

Table 10 : Bank 1 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BG25 | LPDDR4_1_CH1_DQ_A[11] |
| BF25 | LPDDR4_1_CH1_DQ_A[10] |
| BG27 | LPDDR4_1_CH1_DQS_C_A[1] |
| BF27 | LPDDR4_1_CH1_DQS_T_A[1] |
| BJ27 | LPDDR4_1_CH1_DQ_A[14] |
| BH27 | LPDDR4_1_CH1_DQ_A[15] |
| BK27 | LPDDR4_1_CH1_DQ_A[13] |
| BK26 | LPDDR4_1_CH1_DQ_A[12] |
| BR24 | LPDDR4_1_CH0_DQ_B[0] |
| BR23 | LPDDR4_1_CH0_DQ_B[1] |
| BU23 | LPDDR4_1_CH0_DMI_B[0] |
| BU24 | LPDDR4_1_CH0_DQ_B[3] |
| BT24 | LPDDR4_1_CH0_DQ_B[2] |
| BV25 | LPDDR4_1_CH0_DQ_B[4] |
| BV24 | LPDDR4_1_CH0_DQ_B[5] |
| BN27 | LPDDR4_1_CH1_DQS_C_B[1] |
| BM26 | LPDDR4_1_CH1_DQS_T_B[1] |
| BP26 | LPDDR4_1_CH1_DQ_B[10] |
| BP25 | LPDDR4_1_CH1_DQ_B[11] |
| BT25 | LPDDR4_1_CH1_DQ_B[8] |
| BR25 | LPDDR4_1_CH1_DQ_B[9] |
| BR27 | LPDDR4_1_CH1_DMI_B[1] |
| BV28 | LPDDR4_1_CH1_CK_C_A[0] |
| BU28 | LPDDR4_1_CH1_CK_T_A[0] |
| BR29 | LPDDR4_1_CH1_DQ_A[5] |
| BR28 | LPDDR4_1_CH1_DQ_A[4] |
| BT30 | LPDDR4_1_CH1_DQ_A[3] |
| BR30 | LPDDR4_1_CH1_DQ_A[2] |
| BG32 | LPDDR4_1_CH1_CK_C_B[0] |
| BG31 | LPDDR4_1_CH1_CK_T_B[0] |
| BH31 | LPDDR4_1_CH1_CA_B[3] |
| BH30 | LPDDR4_1_CH1_CA_B[4] |
| BJ29 | LPDDR4_1_CH1_CA_B[1] |
| BJ28 | LPDDR4_1_CH1_CA_B[0] |
| BJ32 | LPDDR4_1_CH1_CKE_B[0] |
| BJ31 | LPDDR4_1_CH1_CKE_B[1] |

Table 10 : Bank 1 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BL32 | LPDDR4_1_CH1_CA_B[2] |
| BK33 | LPDDR4_1_CH1_CA_B[5] |
| BE29 | LPDDR4_1_CH1_DQS_C_B[0] |
| BE28 | LPDDR4_1_CH1_DQS_T_B[0] |
| BE32 | LPDDR4_1_CH1_DQ_B[4] |
| BE31 | LPDDR4_1_CH1_DQ_B[5] |
| BU29 | LPDDR4_1_CH1_CA_A[5] |
| BT29 | LPDDR4_1_CH1_CA_A[4] |
| BG33 | LPDDR4_1_CH1_DQ_B[3] |
| BF33 | LPDDR4_1_CH1_DQ_B[2] |
| BF31 | LPDDR4_1_CH1_CS_B[1] |
| BF30 | LPDDR4_1_CH1_DMI_B[0] |
| BG28 | LPDDR4_1_CH1_DQ_B[6] |
| BF28 | LPDDR4_1_CH1_DQ_B[7] |
| BH29 | LPDDR4_1_CH1_DQ_B[0] |
| BG29 | LPDDR4_1_CH1_DQ_B[1] |
| BT32 | LPDDR4_1_CH1_CS_A[1] |
| BR32 | LPDDR4_1_CH1_CKE_A[0] |
| BU32 | LPDDR4_1_CH1_CKE_A[1] |
| BT31 | LPDDR4_1_CH1_CS_A[0] |
| BV31 | LPDDR4_1_CH1_CA_A[0] |
| BU31 | LPDDR4_1_CH1_CA_A[1] |
| BV30 | LPDDR4_1_CH1_CA_A[2] |
| BV29 | LPDDR4_1_CH1_CA_A[3] |
| BN29 | LPDDR4_1_CH1_CS_B[0] |
| BM29 | LPDDR4_1_CH1_DMI_A[0] |
| BM31 | LPDDR4_1_CH1_DQ_A[7] |
| BM30 | LPDDR4_1_CH1_DQ_A[6] |
| BN32 | LPDDR4_1_CH1_DQ_A[0] |
| BN31 | LPDDR4_1_CH1_DQ_A[1] |
| BP31 | LPDDR4_1_CH1_DQS_C_A[0] |
| BP30 | LPDDR4_1_CH1_DQS_T_A[0] |

Table 10 : Bank 1

| Pin Number | Signal Name |
|------------|-------------------------|
| BL33 | REFCLK_MEM2_P |
| BM33 | REFCLK_MEM2_N |
| BT36 | LPDDR4_2_CH0_CS_B[0] |
| BT35 | LPDDR4_2_CH0_DMI_B[1] |
| BR35 | LPDDR4_2_CH0_DQ_A[12] |
| BR34 | LPDDR4_2_CH0_DQ_A[10] |
| BT34 | LPDDR4_2_CH0_DQ_A[11] |
| BR33 | LPDDR4_2_CH0_DQ_A[9] |
| BH35 | LPDDR4_2_CH0_CK_C_B[0] |
| BH34 | LPDDR4_2_CH0_CK_T_B[0] |
| BH38 | LPDDR4_2_CH0_CA_B[4] |
| BH37 | LPDDR4_2_CH0_CA_B[5] |
| BJ37 | LPDDR4_2_CH0_CA_B[1] |
| BJ36 | LPDDR4_2_CH0_CKE_B[0] |
| BL35 | LPDDR4_2_CH0_CKE_B[1] |
| BK35 | LPDDR4_2_CH0_CA_B[0] |
| BK38 | LPDDR4_2_CH0_CA_B[2] |
| BK37 | LPDDR4_2_CH0_CA_B[3] |
| BE37 | LPDDR4_2_CH0_CK_C_A[0] |
| BD36 | LPDDR4_2_CH0_CK_T_A[0] |
| BE35 | LPDDR4_2_CH0_CA_A[5] |
| BD35 | LPDDR4_2_CH0_CA_A[4] |
| BV38 | LPDDR4_2_CH0_DQ_B[15] |
| BU38 | LPDDR4_2_CH0_DQ_B[13] |
| BE34 | LPDDR4_2_CH0_CKE_A[1] |
| BD33 | LPDDR4_2_CH0_CKE_A[0] |
| BG35 | LPDDR4_2_CH0_CS_A[1] |
| BF34 | LPDDR4_2_CH0_CA_A[2] |
| BG36 | LPDDR4_2_CH0_CA_A[0] |
| BF36 | LPDDR4_2_CH0_CA_A[1] |
| BG37 | LPDDR4_2_CH0_CA_A[3] |
| BF37 | LPDDR4_2_CH0_CS_A[0] |
| BL37 | LPDDR4_2_CH1_RESET_N[0] |
| BL36 | LPDDR4_2_CH0_RESET_N[0] |
| BU37 | LPDDR4_2_CH0_DQ_B[14] |
| BU36 | LPDDR4_2_CH0_DQ_B[12] |

Table 11 : Bank 2 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BV36 | LPDDR4_2_CH0_DQS_C_B[1] |
| BV35 | LPDDR4_2_CH0_DQS_T_B[1] |
| BV34 | LPDDR4_2_CH0_DQ_B[9] |
| BU34 | LPDDR4_2_CH0_DQ_B[8] |
| BV33 | LPDDR4_2_CH0_DQ_B[11] |
| BU33 | LPDDR4_2_CH0_DQ_B[10] |
| BM35 | LPDDR4_2_CH0_DQS_C_A[1] |
| BM34 | LPDDR4_2_CH0_DQS_T_A[1] |
| BP35 | LPDDR4_2_CH0_DQ_A[13] |
| BN35 | LPDDR4_2_CH0_DQ_A[15] |
| BP36 | LPDDR4_2_CH0_DQ_A[14] |
| BN36 | LPDDR4_2_CH0_DQ_A[8] |
| BT37 | LPDDR4_2_CH0_CS_B[1] |
| BR37 | LPDDR4_2_CH0_DMI_A[1] |
| BN40 | LPDDR4_2_CH0_DQS_C_B[0] |
| BN39 | LPDDR4_2_CH0_DQS_T_B[0] |
| BV43 | LPDDR4_2_CH1_DQ_B[8] |
| BU43 | LPDDR4_2_CH1_DQ_B[9] |
| BV44 | LPDDR4_2_CH1_DQ_B[12] |
| BU44 | LPDDR4_2_CH1_DQ_B[14] |
| BE41 | LPDDR4_2_CH0_DQS_C_A[0] |
| BE40 | LPDDR4_2_CH0_DQS_T_A[0] |
| BF39 | LPDDR4_2_CH0_DQ_A[1] |
| BE38 | LPDDR4_2_CH0_DQ_A[0] |
| BG40 | LPDDR4_2_CH0_DQ_A[2] |
| BG39 | LPDDR4_2_CH0_DQ_A[3] |
| BH41 | LPDDR4_2_CH0_DMI_A[0] |
| BJ39 | LPDDR4_2_CH0_DQ_A[5] |
| BH39 | LPDDR4_2_CH0_DQ_A[4] |
| BL39 | LPDDR4_2_CH0_DQ_A[6] |
| BK39 | LPDDR4_2_CH0_DQ_A[7] |
| BF40 | LPDDR4_2_CH1_DMI_A[0] |
| BG43 | LPDDR4_2_CH1_DQ_A[2] |
| BF42 | LPDDR4_2_CH1_DQ_A[0] |
| BR40 | LPDDR4_2_CH0_DQ_B[1] |
| BP40 | LPDDR4_2_CH0_DQ_B[2] |

Table 11 : Bank 2 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BH43 | LPDDR4_2_CH1_DQ_A[3] |
| BH42 | LPDDR4_2_CH1_DQ_A[1] |
| BK41 | LPDDR4_2_CH1_DQS_C_A[0] |
| BJ41 | LPDDR4_2_CH1_DQS_T_A[0] |
| BK43 | LPDDR4_2_CH1_DQ_A[5] |
| BJ43 | LPDDR4_2_CH1_DQ_A[4] |
| BL43 | LPDDR4_2_CH1_DQ_A[7] |
| BK42 | LPDDR4_2_CH1_DQ_A[6] |
| BR39 | LPDDR4_2_CH0_DQ_B[3] |
| BR38 | LPDDR4_2_CH0_DQ_B[4] |
| BT39 | LPDDR4_2_CH0_DMI_B[0] |
| BV39 | LPDDR4_2_CH0_DQ_B[6] |
| BU39 | LPDDR4_2_CH0_DQ_B[5] |
| BV41 | LPDDR4_2_CH0_DQ_B[0] |
| BV40 | LPDDR4_2_CH0_DQ_B[7] |
| BP41 | LPDDR4_2_CH1_DQS_C_B[1] |
| BN41 | LPDDR4_2_CH1_DQS_T_B[1] |
| BR43 | LPDDR4_2_CH1_DQ_B[15] |
| BR42 | LPDDR4_2_CH1_DQ_B[13] |
| BU41 | LPDDR4_2_CH1_DQ_B[10] |
| BT41 | LPDDR4_2_CH1_DQ_B[11] |
| BT42 | LPDDR4_2_CH1_DMI_B[1] |
| BR45 | LPDDR4_2_CH1_CK_C_A[0] |
| BR44 | LPDDR4_2_CH1_CK_T_A[0] |
| BP47 | LPDDR4_2_CH1_DQ_A[10] |
| BP46 | LPDDR4_2_CH1_DQ_A[8] |
| BR48 | LPDDR4_2_CH1_DQ_A[11] |
| BR47 | LPDDR4_2_CH1_DQ_A[9] |
| BJ44 | LPDDR4_2_CH1_CK_C_B[0] |
| BH45 | LPDDR4_2_CH1_CK_T_B[0] |
| BK45 | LPDDR4_2_CH1_CA_B[3] |
| BJ45 | LPDDR4_2_CH1_CA_B[4] |
| BJ48 | LPDDR4_2_CH1_CA_B[1] |
| BJ47 | LPDDR4_2_CH1_CA_B[0] |
| BK50 | LPDDR4_2_CH1_CKE_B[0] |
| BK49 | LPDDR4_2_CH1_CKE_B[1] |

Table 11 : Bank 2 (continued on next page)

| Pin Number | Signal Name |
|------------|-------------------------|
| BL45 | LPDDR4_2_CH1_CA_B[2] |
| BL44 | LPDDR4_2_CH1_CA_B[5] |
| BG45 | LPDDR4_2_CH1_DQS_C_B[0] |
| BG44 | LPDDR4_2_CH1_DQS_T_B[0] |
| BG48 | LPDDR4_2_CH1_DQ_B[7] |
| BG47 | LPDDR4_2_CH1_DQ_B[6] |
| BT45 | LPDDR4_2_CH1_CA_A[5] |
| BT44 | LPDDR4_2_CH1_CA_A[4] |
| BG49 | LPDDR4_2_CH1_DQ_B[0] |
| BF50 | LPDDR4_2_CH1_DQ_B[3] |
| BH50 | LPDDR4_2_CH1_CS_B[1] |
| BG50 | LPDDR4_2_CH1_DMI_B[0] |
| BJ49 | LPDDR4_2_CH1_DQ_B[2] |
| BH49 | LPDDR4_2_CH1_DQ_B[1] |
| BH47 | LPDDR4_2_CH1_DQ_B[5] |
| BH46 | LPDDR4_2_CH1_DQ_B[4] |
| BT47 | LPDDR4_2_CH1_CS_A[1] |
| BT46 | LPDDR4_2_CH1_CKE_A[0] |
| BV48 | LPDDR4_2_CH1_CKE_A[1] |
| BU48 | LPDDR4_2_CH1_CS_A[0] |
| BU47 | LPDDR4_2_CH1_CA_A[0] |
| BU46 | LPDDR4_2_CH1_CA_A[1] |
| BV46 | LPDDR4_2_CH1_CA_A[2] |
| BV45 | LPDDR4_2_CH1_CA_A[3] |
| BN49 | LPDDR4_2_CH1_CS_B[0] |
| BM49 | LPDDR4_2_CH1_DMI_A[1] |
| BN48 | LPDDR4_2_CH1_DQ_A[13] |
| BN47 | LPDDR4_2_CH1_DQ_A[12] |
| BN45 | LPDDR4_2_CH1_DQ_A[14] |
| BM45 | LPDDR4_2_CH1_DQ_A[15] |
| BP45 | LPDDR4_2_CH1_DQS_C_A[1] |
| BN44 | LPDDR4_2_CH1_DQS_T_A[1] |

Table 11 : Bank 2

Appendix B: Backplane HSSIO Quad Mapping

| ACAP Quad | Lane | Signal Name |
|-----------|------|-------------|
| 200 | 0 | CSUTP1 |
| 200 | 1 | CPUTP1 |
| 200 | 2 | CPUTP2 |
| 200 | 3 | CPUTP3 |
| 201 | 0 | CPUTP5 |
| 201 | 1 | CPUTP4 |
| 201 | 2 | CPUTP6 |
| 201 | 3 | CPUTP7 |
| 202 | 0 | DPFP03_DP3 |
| 202 | 1 | DPFP03_DP2 |
| 202 | 2 | DPFP03_DP1 |
| 202 | 3 | DPFP03_DP0 |
| 203 | 0 | DPFP02_DP3 |
| 203 | 1 | DPFP02_DP2 |
| 203 | 2 | DPFP02_DP1 |
| 203 | 3 | DPFP02_DP0 |
| 208 | 0 | DPFP01_DP3 |
| 208 | 1 | DPFP01_DP2 |
| 208 | 2 | DPFP01_DP1 |
| 208 | 3 | DPFP01_DP0 |
| 209 | 0 | DSFP01_DP3 |
| 209 | 1 | DSFP01_DP2 |
| 209 | 2 | DSFP01_DP1 |
| 209 | 3 | DSFP01_DP0 |

Table 12 : Backplane HSSIO Quad Mapping

Appendix C: Optical Mezzanine HSSIO Quad Mapping

| ACAP Quad | Lanes | Signal Name |
|-----------|-------|-------------|
| 104 | [3:0] | OMFP0[3:0] |
| 105 | [3:0] | OMFP1[3:0] |
| 106 | [3:0] | OMFP2[3:0] |
| 107 | [3:0] | OMFP5[0:3] |
| 108 | [3:0] | OMFP4[0:3] |
| 109 | [3:0] | OMFP3[0:3] |

Table 13 : Optical Mezzanine HSSIO Quad Mapping

Revision History

| Date | Revision | Nature of Change |
|--------------------|----------|-------------------------------|
| 29th October 2025 | 0.1 | Initial Draft |
| 10th November 2025 | 0.2 | Updates |
| 11th November 2025 | 0.3 | Further Updates |
| 12th November 2025 | 1.0 | Incorporated review comments. |